

This way of reading the PC is primarily used for quick, position-independent addressing of nearby instructions and data, including position-independent branching within a program.

An exception to this rule occurs when an STR (Store Register) or STM (Store Multiple Registers) instruction stores R15. The value stored is UNKNOWN and it is best to avoid the use of these instructions that store R15.

Writing the program counter

When an instruction writes to R15 the normal result is that the value written is treated as an instruction address and the system starts to execute the instruction at that address³.

3.2.4 Current Processor Status Registers: CPSR

Rather surprisingly the *current processor status register* (CPSR) contains the current status of the processor. This includes various condition code flags, interrupt status, processor mode and other status and control information.

The exception modes also have a *saved processor status register* (SPSR), that is used to preserve the value of the CPSR when the associated exception occurs. Because the User and System modes are not exception modes, there is no **SPSR** available.

Figure 3.4 shows the format of the CPSR and the SPSR registers.

31	30	29	28	27	...	8	7	6	5	4	...	0
N	Z	C	V	SBZ			I	F	SBZ	Mode		

Figure 3.4: Structure of the Processor Status Registers

The processors' status is split into two distinct parts: the User flags and the Systems Control flags. The upper halfword is accessible in User mode and contains a set of flags which can be used to effect the operation of a program, see section 3.3. The lower halfword contains the System Control information.

Any bit not currently used is reserved for future use and should be zero, and are marked SBZ in the figure. The I and F bits indicate if Interrupts (I) or Fast Interrupts (F) are allowed. The Mode bits indicate which operating mode the processor is in (see 3.1 on page 23).

The system flags can only be altered when the processor is in protected mode. User mode programs can not alter the status register except for the condition code flags.

3.3 Flags

The upper four bits of the status register contains a set of four flags, collectively known as the *condition code*. The condition code flags are:

Negative	(N)
Zero	(Z)
Carry	(C)
Overflow	(V)

³ As the processor has already fetched the instruction after the current instruction it is required to flush the instruction cache and start again. This will cause a short, but not significant, delay.