operation dictates the filter capacitor requirements.

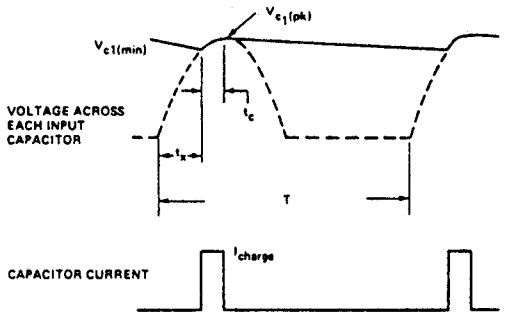

Figure 4. Voltage Doubler Charging Current

Figure 4 shows the waveforms associated with charging each of the input capacitors in the voltage doubler configuration at full load and minimum line voltage. Recharge time, t_c, is established by the intercept of the capacitor voltage waveform with the rectified AC line:

$$V_{C1min} = V_{C1pk} \cos(2\pi f\, t_c)$$

$$t_c = \frac{\cos^{-1}(V_{C1min}/V_{C1pk})}{2\pi f} \qquad (9)$$

$$t_c = \frac{\cos^{-1}(88.3/135)}{2\pi\ 60} = \qquad 2.275 \text{ ms}$$

Assuming a rectangular charging current pulse of peak amplitude ichg (constant current during the charging interval):

$$\Delta Q = i_{chg}\,\Delta t = C\,\Delta V$$

$$i_{chg} = C\,(V_{pk} - V_{min})/t_c \qquad (10)$$

$$i_{chg} = 160(135-88.3)/2.275 \times 10^{-3} = \qquad 3.28 \text{ A}$$

The RMS current in each capacitor is:

$$I_{chg} = i_{chg}\sqrt{t_c f - t_c f^2} \qquad (11)$$

$$t_c f = 2.275\times10^{-3}\ 60 = .1365$$

$$I_{chg} = 3.28\sqrt{.1365 - .1365^2} = \qquad 1.126 \text{ A}$$

High Power Factor Preregulators for Off-Line Power Supplies

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hpf.wp

Introduction

Off-line switching power supplies usually employ a rectifier bridge or doubler with a simple capacitor input filter to draw power from the ac line. The "bulk" filter capacitor charges to nearly the peak ac line voltage, supporting an unregulated dc bus powering the downstream switching converters. This bulk capacitor must be *large*. It alone supplies total power during most of each half-cycle while instantaneous line voltage is below the dc bus, (or for longer time, depending on hold-up requirements).

Unfortunately, with a capacitor input filter, the line current waveform is non-sinusoidal—a narrow pulse with very high peak current. Input power factor is only 0.5 – 0.65 and the high harmonic content causes line noise. The rms line current may be twice the equivalent rms sine wave. A 120V, 15A line may not be able to supply even 1 kW of input power without tripping the line circuit breaker. With lower wattage systems, perhaps twice as many high power factor supplies could operate from the same line. For these reasons, high power factor is becoming a requirement in many power supply specifications.

The high power factor switching preregulators described in this paper are interposed between the input rectifier bridge and the bulk filter capacitor. Switching at a frequency *much* higher than the line, the preregulator is programmed to draw a half-sinusoid input current, in phase with the line voltage. The current is controlled by the deviation of the dc bus voltage from the desired value. The result is:

1. Improved input power factor: .95 to .999
2. Reduced harmonics ($i_{rms} \leq 3\%$, if necessary)
3. Tapless/switchless operation over the full 90V – 270V line voltage range.
4. Crudely regulated bulk capacitor voltage. The resulting narrow dc bus voltage range permits the downstream converters to be designed for lower cost and greater reliability and efficiency.
5. Smaller bulk capacitor size and cost.
6. Reduced rms charging current resulting in improved capacitor reliability.

Basic Preregulator Operation

Throughout this paper, a preregulator switching frequency, f_s = 100 kHz, and a line frequency, f_L = 60 Hz are assumed.

Referring to Fig. 1, to achieve an input power factor approaching 1.0, the preregulator is programmed to draw input current which varies in direct instantaneous proportion to the input voltage half sine wave. Thus the voltage and current waveforms on the input side of the rectifier bridge are in-phase sine waves. This is of course what a simple resistive load does, and an active preregulator circuit performing this function is often called a "resistor emulator".

The input current programming signal may be obtained by multiplying a half-sinusoid

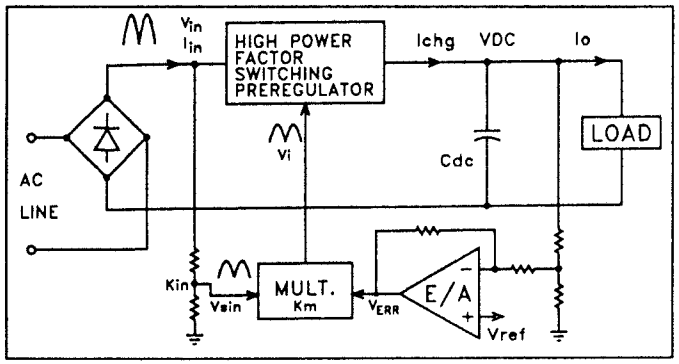


Fig. 1 - High Power Factor Preregulator

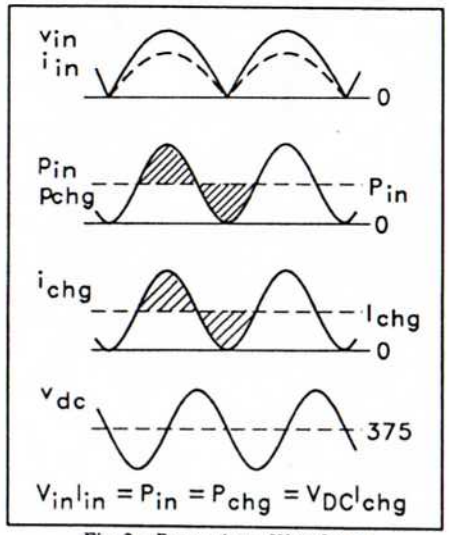


Fig. 2 - Preregulator Waveforms

(usually derived from the rectified line voltage waveform) by a control voltage, V_{ERR}, which must be constant during each half-cycle. Thus V_{ERR} controls the rms input current, governing the power drawn from the line during each half cycle. V_{ERR} represents the deviation of V_{DC} from its desired value, amplified and inverted at the error amplifier output. When V_{DC} is low, V_{ERR} is large, calling for increased input power to make up the energy deficit in the bulk filter capacitor, C_{DC}, across the dc bus.

Power transfer: Although the preregulator input current waveform is a half-sinusoid, its output current i_{chg}, which charges C_{DC}, is a sine squared function (see Fig. 2). Considerable operational insight can be gained by thinking in terms of the preregulator *power input* and *power output*, rather than input/output voltages and currents—see Fig. 2. Assuming the preregulator operates with high efficiency and at a switching frequency very much greater than the line (100 kHz vs. 50-60 Hz), the amount of energy stored or dissipated within the preregulator can be considered negligible at the line frequency. (Inductive energy stored in the preregulator is usually more than the energy transferred during one *switching* frequency cycle, but totally negligible compared to energy transfer during one *line* half-cycle.) Thus on a time scale relevant to the line frequency, the instantaneous power output to C_{DC} equals the power input, and the cumulative energy delivered to C_{DC} during each line half-cycle equals the energy drawn from the line.

With high power factor (1.0), the line voltage and current waveforms are in-phase sine waves, by definition. Thus, during each half-cycle, the instantaneous input power, p_{in}, (and p_{chg}, the power output to C_{DC}) is a $\sin^2$ function:

$$p_{chg} = p_{in} = 2\,V_{in}I_{in}\sin^2\omega_L t \qquad (1)$$

where V_{in} and I_{in} are rms values and $\omega_L = 2\pi$ times line frequency.

Since $2\sin^2 x = 1 - \cos 2x$, then

$$p_{chg} = p_{in} = V_{in}I_{in}(1 - \cos 2\omega_L t) \qquad (2)$$

C_{DC} is usually large enough to hold the dc bus voltage V_{DC} fairly constant. Thus the charging current is nearly proportional to the instantaneous power, and:

$$i_{chg} \approx p_{chg}/V_{DC}$$

$$\approx V_{in}I_{in}(1 - \cos 2\omega_L t)/V_{DC} \qquad (3)$$

$$I_{CHG} = V_{in}I_{in}/V_{DC} \qquad (4)$$

(4) is the average of (3)

As shown in Fig. 2, the ac component of i_{chg} produces a small ripple voltage, v_{dc}, at $2f_L$ (with 90° phase lag) on the dc bus, depending on capacitor size. i_{chg} is not perfectly sinusoidal because the ripple component of V_{DC} makes Eq. 3 an approximation, but the error is negligible in practice.

For a minimal C_{DC} value (providing ⅓ cycle hold-up), the ripple voltage on a 400 V dc bus will be approximately 10 to 20 Vp-p at full load. If C_{DC} is too small, the dc bus ripple voltage will be larger, but more importantly, bus voltage regulation against line and load changes will be very poor and hold-up capability will be inadequate.

Note that in the entire preceding discussion, the specific power circuit topology was not mentioned. Indeed, the input/output voltage, current and power waveforms and magnitudes are fundamental to the preregulator's task of maintaining good input power factor, charging C_{DC} and regulating the dc bus voltage, totally independent of the specific power circuit used.

Power Circuit Topology

Three basic power circuit topologies—Buck, Flyback, and Boost—that might be used in the high power factor switching preregulator are shown in Fig. 3. Each circuit has its advantages and disadvantages which are summarized in Fig. 4.

Boost topology: This is the most popular HPFP configuration. Boost circuits require that the output voltage, V_{DC}, must always be greater than instantaneous line voltage, v_{in}. A boost circuit designed for a V_{DC} level exceeding the maximum peak line voltage can operate over the full line voltage range, from zero to the max. peak value. V_{DC} of 380–400V allows operation over a span of 90V to 270V rms line without range switching. However, because V_{DC} must exceed v_{in}, the boost topology is not compatible with a standard 300 V_{DC} bus from a 220V line. Unfortunately, a 400V bus requires higher voltage ratings for the devices used in the downstream converters.

In the boost configuration, the input current is not switched and di/dt is low because of the inductor location. This minimizes line noise and EMI. In addition, line spikes are absorbed by the inductor, increasing circuit reliability.

With continuous mode operation, the input location of the inductor also makes it easy to use current mode control to program the input current half sine. (Current mode control actually controls inductor current.)

The circuit location of the transistor switch makes it easy to drive the gate/base, since the source/emitter is referenced to the control circuit and C_{DC} common. The maximum voltage applied to the transistor equals the output voltage, V_{DC}.

Probably the greatest disadvantage of the boost topology is its *inability to limit current*, because there is no series switch between input and output. Overload or startup overcurrent conditions cannot be controlled or limited. While it can be argued that the downstream switching power converters will provide the necessary current limiting to protect the preregulator, failure of the bulk capacitor or converter transistors is not covered.

Furthermore, the boost topology can not function with V_{DC} less than the instantaneous line voltage. This occurs every time the supply

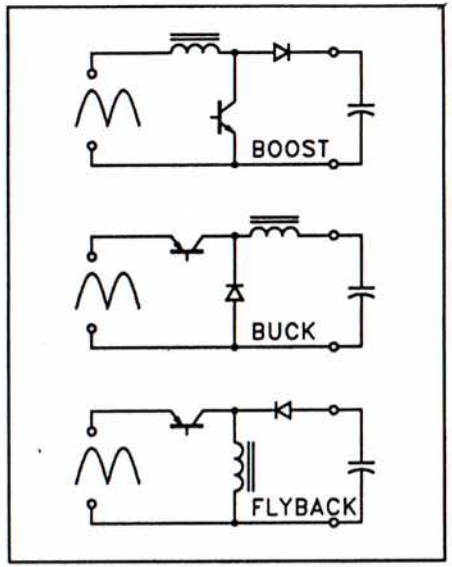


Fig. 3 - Basic Preregulator Topologies

is turned on, and after line voltage interruptions of sufficient duration. Soft start is useless because the boost circuit does not function under these conditions. The transistor switch will remain *off*, but input current will rise to a peak value several times greater than normal maximum levels, saturating the input inductor and causing failure unless *additional* current limiting circuits are provided. This will be discussed fully later in this paper.

Slope compensation is required with continuous mode operation to avoid instability at duty ratios > 0.5, occurring whenever instantaneous v_{in} is less than $V_{DC}/2$. Slope compensation is difficult to accomplish with the boost topology because the inductor current downslope (which determines the compensation required) varies considerably with v_{in}. This problem can be avoided by reducing the bandwidth of the inner current control loop so that the *average* inductor current is directly controlled, rather than the *peak* current intercept. There is plenty of room to reduce the current loop bandwidth without affecting circuit performance because the switching frequency is so much higher than the line frequency.

BOOST - Constant Frequency, Continuous Mode

ADVANTAGES:
1. Input current is not chopped - little EMI
2. Inductor current *is* input current - current mode control is ideal to program input current waveform.
3. Switch voltage ratings = V_o
4. Inductor at input absorbs line voltage spikes
5. Easy to drive switch - source/emitter at zero ref.

DISADVANTAGES:
1. No control when $V_{in} > V_o$ - start-up, line overvoltage
2. Cannot limit overcurrent - load fault, start-up.
3. V_o higher than max. peak V_{in} requires higher voltages in downstream converter.
4. Slope compensation required - changes with V_{in}

BUCK

Unsuitable for high power factor preregulator except as supplement to Boost preregulator for current limiting.

FLYBACK - Constant Frequency, Continuous Mode.

ADVANTAGES:
1. V_o can be greater or less than peak V_{in}
   a. 300V bus - eases voltage requirements of downstream converter.
   b. Can control start-up current inrush and load fault.
2. Easy to provide isolation in preregulator rather than in downstream converter transformers.

DISADVANTAGES:
1. High switch voltage ratings: $V_o + V_{in}$
2. Chopped input current - hard to filter - EMI
3. Difficult to program input current half sine with current mode control
4. Slope compensation required

Discontinuous Flyback – PRO'S & CON'S
1. Automatic current half-sine by programming and fixing the "on" time during each line half-cycle.
2. No slope compensation required.
3. Peak current nearly twice continuous mode flyback

Fig. 4 - Preregulator Topology Advantages/Disadvantages

The discontinuous inductor current mode is impractical for the boost topology in the high power factor preregulator because at peak V_{in} the inductor current downslope is very shallow, so ripple current is small. But in a high power factor preregulator at peak V_{in}, line current is at its peak. With high peak current but low ripple, inductor current must be continuous.

Buck Topology: In the buck configuration, V_{in} must be greater than V_o. This makes it unsuitable for high power factor preregulator use because it cannot function on the skirts of the input half sine when v_{in} is less than V_{DC}. However, the buck topology can be very useful to provide current limit support to a boost preregulator.

Flyback Topology: The flyback (buck-boost) configuration overcomes two of the boost topology disadvantages: The flyback circuit can control and limit start-up inrush current and load overcurrent. Also, the output voltage may be *greater or less* than the instantaneous input voltage, making it possible to provide a 300V bus from a 220V rms line.

In the basic flyback circuit, output voltage must be opposite in polarity from the input voltage. This may be inconvenient. But the circuit location of the inductor provides a unique possibility for the flyback: the inductor could have primary and secondary windings. This can provide polarity independence and also input-output isolation in the preregulator, relieving the downstream converters of this isolation requirement. The converter transformers can be simplified and leakage inductance reduced because creepage and insulation are eliminated. Isolated feedback can also be eliminated in the downstream converters, making it easy and inexpensive to achieve good regulation.

However, the chopped input waveform of the flyback circuit results in more noise and EMI than the comparable boost topology, requiring more input filtering.

The location of the transistor switch makes it difficult to drive the gate/base—a small drive transformer is normally used.

The transistor voltage rating must be greater than max peak $v_{in} + V_{DC}$, much higher than with the boost configuration.

Finally, it is more difficult to program the required input current half-sine wave with the flyback preregulator and current mode control. This is because current mode control actually controls *peak inductor* current, which is almost the same as the *average inductor* current with continuous mode operation (with any topology). The inductor current *is* the input current in the boost topology, but not in flyback circuits. The relationship between flyback input current and inductor current changes considerably with v_{in}, which complicates input current programming. Also, slope compensation is required with continuous mode operation.

Both of the above problems can be overcome by using *average input* current mode control, sacrificing some current loop bandwidth, as discussed earlier with the boost circuit.

Discontinuous mode flyback: Input current can be easily programmed in the constant frequency, discontinuous operating mode if the "on" time, or duty ratio, is made proportional to the control voltage, V_{ERR}. Peak and average currents at 100 kHz will then be proportional to the instantaneous line voltage waveform, automatically providing high power factor during each half cycle. No slope compensation is required with discontinuous operation.

The main disadvantage of the discontinuous mode is that the triangular shaped input waveform has nearly twice the peak current of the comparable continuous mode waveform. This increases noise problems and transistor current rating requirements.

The Control Loop

The basic control circuit as shown in Fig. 1 is independent of the specific power circuit topology used. It involves an inner current control loop and an outer voltage control loop. The current in the inner loop is programmed according to the output voltage error sensed and amplified by the outer loop. Thus the control circuit operates exactly like any current mode control system—with two exceptions:
1. The current control loop programs the *input* current, not the output current.
2. The programmed current is proportional to the control voltage, V_{ERR}, *multiplied by a half sine derived from the rectified line voltage.*

These two control system elements assure that the input current is a half sine wave in phase with the rectified input voltage, i.e., the input power factor approaches 1.0.

However, there are several significant and limiting problems with this basic control system approach. To set the stage for this, consider the following:

The load power demand on the switching preregulator does not change with input rms line voltage, for two reasons:
1. The preregulator maintains a fairly constant output bus voltage V_{DC}.
2. The downstream switching converters draw constant power regardless of V_{DC} variation.

Since the switching preregulator operates with high efficiency, the *input power drawn from the line does not change with rms line voltage*, but only with downstream load changes.

Therefore, when rms line voltage varies:

a. *rms* line current must be *inversely proportional* to the *rms* line voltage to maintain constant power input.

But *within each half-cycle*:

b. *Instantaneous* current must be *directly proportional* to *instantaneous* line voltage in order to have a good power factor.

Poor open loop line regulation: Criteria (a) and (b) above conflict with each other in the basic control circuit. If control voltage V_{ERR} is fixed (open control loop), instantaneous current programmed by the multiplier is directly proportional to instantaneous line voltage, thus satisfying (b) and providing good power factor. However, in contradiction to (a), rms line current will also vary *directly* with rms line voltage. Thus, although power input should not change, it will actually vary with the *square* of the rms line voltage. This results in very poor open loop line regulation, and requires strong closed loop intervention to correct. But it will be shown that the control loop bandwidth must be much less than 120 Hz. This causes considerable change in dc bus voltage when the line voltage changes rapidly. Without current limiting, input current may be excessive for several half-cycles.

The usual solution to this problem caused by low bandwidth is to add considerable additional control circuitry to sense and limit input current and/or power and to sense and limit over and under-voltage on the dc bus. These auxiliary circuits override the slow main control loop to achieve quick corrective intervention. Whenever this occurs, the input waveform is clipped and the power factor is low for several half-cycles while the main control loop slowly adapts to the new conditions.

A much better solution uses *input voltage feed-forward* to provide the main control circuit with good inherent open-loop line regulation. With input voltage feed-forward, the control circuit can respond to a line voltage change within one half cycle, maintaining low power factor and eliminating most of the additional control circuitry.

Control loop bandwidth limitation: As discussed previously, with a bulk filter capacitor of acceptable cost and size, there will be 120 Hz ripple voltage on the dc bus, perhaps $10V_{p\text{-}p}$ on a 380V bus at full load. This results in a 120 Hz control voltage component at the error amplifier output, which will oppose and reduce the ripple on the dc bus, depending upon the control loop gain at 120 Hz. While this ripple reduction is a laudable goal, the 120 Hz control voltage component will distort the half-sine current programming waveform and the input current, as shown in Fig. 5. This can make it impossible to achieve the desired power factor.

To prevent this distortion, *the control voltage must not be allowed to change significantly during each line half-cycle.* Control loop bandwidth must be much less than 120 Hz to keep the input sine wave distortion to an acceptable level. Circuit simulation shows that to achieve P.F. = .96, *the maximum* crossover frequency, f_c, is about 20 Hz at max. V_{in}. At lower V_{in}, f_c will be *much* less. This low bandwidth severely impairs the control loop dynamics. The dc bus voltage will respond very slowly to line or load changes,making it difficult to keep the dc bus voltage within desired limits. If a power factor greater than .98 is required, control loop bandwidth must be very low. (3% harmonic distortion requires P.F. = .999)

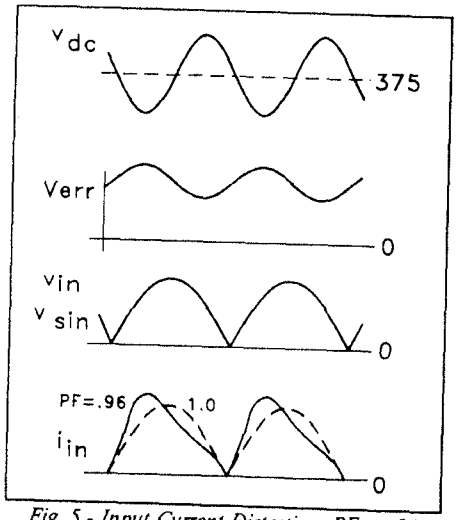


Fig. 5 - Input Current Distortion, PF = .96

Another technique that totally eliminates input current waveform distortion, achieving very high power factors without requiring extreme low bandwidth, is to *sample and hold* the control voltage, V_{ERR}, every half cycle when the line voltage crosses zero. Although the power factor is excellent with the sample and hold (S/H) technique, the crossover frequency is limited to about 20 Hz (one fifth the 120 Hz sampling frequency) for stability reasons.

So whether or not S/H is used, to maintain the dc bus voltage within desired limits requires either (a) extensive override control circuits or (b) input voltage feed-forward, which greatly improves the dynamics by making fast open-loop correction for line voltage changes.

Control loop gain and bandwidth variation: As shown in Eq. (5), the small signal gain from control to output (part of the overall voltage control loop gain) varies with the *square* of the rms input voltage:

$$\frac{v_{dc}}{v_{ERR}} = \frac{kV_{in}^2/V_{DC}}{j\omega C_{DC}} \qquad (5)$$

Thus, the loop gain with V_{in} = 90V is only 1/9 (-19dB) of the loop gain with V_{in} = 270V.

The crossover frequency f_c is also directly proportional to the gain because the gain characteristic has a single pole (-20dB/decade) slope through crossover. Therefore f_c at 90V is also 1/9 of f_c at 270V.

Consider the difficulty covering this span of input voltages (the combined 120V – 220V range limits) without tap switching. The error amplifier gain is set to obtain f_c = 20 Hz maximum crossover frequency at the 270V high line. (A much higher f_c is desired but not possible because of input current distortion.) If the supply is then operated at the 90V low line condition, f_c drops to only 2.2 Hz. Control dynamics become unacceptable. The dc bus voltage, V_{DC}, drops well below the desired regulation range at 90V input because the low frequency loop gain is inadequate.

Again, the proper application of line voltage feed-forward can make the loop gain independent of line voltage variation. This makes it easy to achieve 90V – 270V operation with good dynamics and good dc bus regulation without range switching.

Power/current limit variation: The relatively slow control loop is unable to keep pace with rapid line or load changes. If load power increases rapidly, the control circuit will belatedly try to make up the energy deficit in C_{DC} by drawing excessive current and power from the line for several half-cycles, unless limiting circuitry is provided. Otherwise, line current limits are violated, device current ratings may be exceeded, and excessive power can cause the dc bus voltage to overshoot.

The peak input current is naturally limited because the current programming voltage is clamped by the output voltage capability of the multiplier. The design should set this current programming limit so that 110 - 120% of full load power can be drawn from the line under minimum line voltage conditions.

When the line voltage is high, a fixed current limit allows excessive power input, and dc bus voltage will overshoot with line or load change. A fixed power limit requires the rms current limit to vary *inversely* with V_{in}. This is hard to accomplish without voltage feed-forward.

For example, for the same maximum power, max. rms input current I_{in} should be only 1/3 as much with 270V input as with 90V. But if the peak current limit is set for max. I_{in} needed at 90V, I_{in} at 270V actually increases 30%. This is because V_{sin} at the multiplier input calls for 3 times *larger* current, but the waveform at the multiplier output is clipped at the *peak* input current limit, becoming rectangular in waveshape. Thus the power limit is 4 times larger at 270 V than at 90 V line.

This situation is obviously intolerable, even with a much more limited input voltage range. Additional, rather elaborate control circuits are required to limit current and power, unless input voltage feed-forward is used.

Input Voltage Feed-Forward

It should be apparent by now that input voltage feed-forward is almost a panacea in eliminating a variety of serious problems inherent in the basic high power factor preregulator.

First, without feed-forward, the circuit of Fig. 1 applies voltage V_{sin}, derived from the line input, to one input of the multiplier. This generates a half sine voltage, V_i, patterned after the line voltage waveform and proportional to the amplified output error voltage, V_{ERR}. V_i programs the input current half sine.

$$V_i = k_m V_{sin} \cdot V_{ERR} = k_m k_{in} V_{in} \cdot V_{ERR} \qquad (7)$$

where k_m is the multiplier gain factor, and k_{in} is the input voltage divider ratio.

The current control loop (part of the preregulator block in Fig. 1) establishes I_{in} according to programming voltage V_i and current sense resistor R_{sense}. Vi is attenuated by factor k_i (which equals R_1/R_2 in Fig. 7).

$$I_{in} = k_i V_i / R_{sense}$$

Combining with (7) and let $k_1 = k_m k_{in} k_i$:

$$I_{in} = k_1 V_{in} \cdot V_{ERR} / R_{sense} \qquad (8)$$

Assuming reasonably high power factor, with rms values:

$$P_{chg} = P_{in} = I_{in} V_{in} = k_1 V_{in}^2 V_{ERR} / R_{sense} \qquad (9)$$

the instantaneous version:

$$p_{chg} = k_1 V_{in}^2 (1 - \cos 2\omega_m t) V_{ERR} / R_{sense} \qquad (9a)$$

Eq. (9) shows clearly that "gain" P_{chg}/V_{ERR} varies with V_{in}^2, causing all of the problems mentioned earlier. It also points the way to apply input voltage feed-forward to eliminate this V_{in}^2 dependency: divide Eq. (9) by a voltage proportional to rms V_{in}^2, thus cancelling the V_{in}^2 term in the numerator, as in Eq. (10). The method of implementation is shown in the block diagram of Fig. 6., where terms are defined.

From (9) with the divider added:

$$P_{chg} = \frac{k_1 k_d V_{in}^2 V_{ERR}}{k_s k_f^2 V_{in}^2 R_{sense}} = \frac{k_1 k_2 V_{ERR}}{R_{sense}} \qquad (10)$$

where $k_d/(k_s k_f^2 V_{in}^2)$ = divider gain
$k_2 = k_d/(k_s k_f^2)$

The feed-forward voltage must be *constant* during each half cycle. This fixes the divider gain during the half cycle in inverse proportion to V_{in}^2 to make the overall loop gain and bandwidth independent of V_{in}. But voltage $V_{sin} = k_{in} V_{in}$ applied to the multiplier is a half sine wave to serve as a pattern to obtain the desired high power factor current waveform.

It must be noted that any 120 Hz ripple in the feed-forward voltage applied to the divider will effectively add to the 120 Hz ripple from the error amplifier to increase the input current waveform distortion, reducing the power factor.

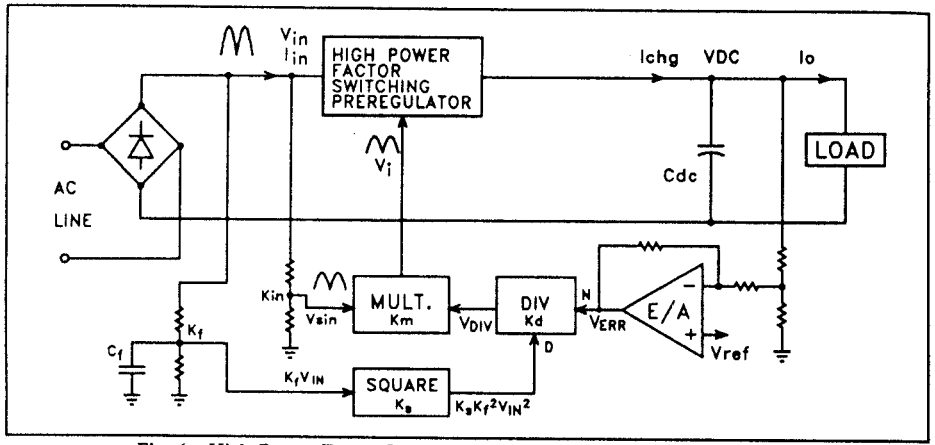


Fig. 6 - High Power Factor Preregulator with Input Voltage Feed-Forward

Capacitor C_f averages the V_{in} waveform and reduces the ripple to an acceptable level. If the time constant $C_fR_{divider}$ is too small, the power factor will be too low. If the time constant is too large, there will be too much feedforward delay, resulting in excessive overshoot and undershoot of the dc bus voltage when the line voltage changes rapidly by a large amount. This is a difficult problem to analyze mathematically, but computer simulation (which is an effective aid for high power factor circuit design) shows that a time constant of one cycle (16 msec at 60 Hz) results in only 4 V overshoot with an instantaneous line change from 180 to 270V, yet is able to achieve a power factor better than .96.

Current Mode Control Problems

Current mode control in its usual implementation is actually "peak inductor current control". When the ripple current is small, the peak inductor current is nearly equal to the average current, which is the actual control objective.

In high power factor preregulator applications, it is desired to control input current. The boost configuration is ideal for current mode control because boost inductor current *is* input current. But buck or flyback circuits are *not* ideal for input current mode control because their inductors are located elsewhere.

(In conventional switching voltage regulator applications, current mode control of *output* current is desired. The buck regulator topology is ideal in this case because the inductor is in the output. But continuous boost and flyback topologies are not well suited because their inductors are not in the output.)

Current mode works by turning off the transistor switch at the point where a voltage derived from the inductor current up-ramp intercepts a relatively constant current programming voltage level. Thus, peak inductor current is controlled. The error between peak and average current is minimized if the ripple current is small but this means the current ramp is shallow and this makes current mode control very noise sensitive.

When current mode control is used in any continuous mode application, slope compensation must be used to ensure stability when duty ratios exceed 0.5. With the boost topology in a high power factor preregulator, slope compensation is needed when the instantaneous line voltage is less than half the output dc bus volts, which occurs for a substantial portion of each line cycle. It is very difficult to achieve slope compensation with the boost preregulator. The inductor current downslope (which determines the amount of slope compensation required) varies with V_{in}, and V_{in} varies tremendously from zero to its large peak value during every line cycle.

Average Current Mode Control

Middlebrook shows that with conventional current mode control, the current loop bandwidth is 1/6 - 1/3 of the switching frequency, f_s. For f_s of 100 kHz, the current loop crossover frequency, f_{ci} > 15 kHz. In conventional voltage regulator applications, this high bandwidth current loop causes the inductor to "disappear" from the small signal model and permits exceptionally high gain-bandwidth in the outer voltage control loop.

But in the high power factor preregulator, the outer loop crossover frequency, f_{co} is limited to less than 20 – 30 Hz, by loop stability or waveform distortion considerations. This means current loop bandwidth f_{ci} does not really need to be more than 1 kHz.

Taking advantage of the wide frequency separation between f_s and f_{co}, the crossover frequency of the current control loop, f_{ci}, is purposely reduced so that the switching frequency ripple and switching noise is reduced to a negligible level. The duty ratio is controlled by comparing the averaged input current error against a sawtooth waveform.

Fig. 7 shows the inner "average current mode control" loop. The input current signal is compared to the 120 Hz current programming voltage V_i (from the multiplier in the outer loop). 100 kHz variations are averaged out through a current error amplifier. The amplified average current error is compared to sawtooth ramp V_s. The comparator output determines the duty ratio of the boost transistor switch which thereby controls the current.

Design approach: The current programming voltage V_i is limited by the multiplier's output voltage swing. This in turn limits the peak input current. The peak voltage across R_{sense} is set by resistor ratio R_1/R_2. For example, suppose a max rms I_{in} of 5 A is desired. If R_{sense} = 0.2 Ω, its dissipation is 5 W, and its voltage is 1 V rms, or 1.414 Vpk. If V_i is limited to 3.0 V, an R_1/R_2 ratio of 1.5/3 = 1/2 establishes a peak input current of 7.5 A, with rms of 5.3 Amps.

To achieve current loop stability, the error amplifier gain, $k_e = R_z/R_i$, is flat from below crossover frequency f_{ci} to above the switching frequency, f_s. This is because a -1 slope (from the inductor) already exists at f_{ci}.

The E/A gain at f_s should be such that the 100 kHz ripple and noise at the E/A output is only one tenth the 3 V sawtooth amplitude, hence negligible. Assuming that inductor L = 700 μH and max Δi_{in} = 1 A have been previously determined, then for example:

$$k_e = \frac{R_z}{R_i} = \frac{V_s/10}{\Delta i_{in} R_{sense}} = \frac{3V/10}{1A \cdot 0.2\Omega} = 1.5 \quad (11)$$

Since the loop gain rolls off with a single pole between f_{ci} and f_s, the resulting crossover frequency is:

$$f_{ci} = \frac{V_o\, k_e R_{sense}}{2\pi L\, V_s} = \frac{380 \cdot 1.5 \cdot 0.2}{2\pi \cdot 700 \cdot 3} = 8.6 \text{ kHz} \quad (12)$$

Zero R_zC_z below $f_{ci}/3$ boosts low frequency gain to "average" the current feedback signal, leaving 45° phase margin at f_{ci}.

Some insights: The "average current control" loop operates in the same manner as old fashioned "voltage mode control", except that it: (a) controls current and (b) functions as the inner loop of a two-loop system. Note that the chopped input current in flyback or buck topologies can be averaged and controlled in the same manner. Average current mode control can be applied to any topology even when the inductor current is not equal to the input current. This makes the specific power circuit topology irrelevant to the outer control loop.

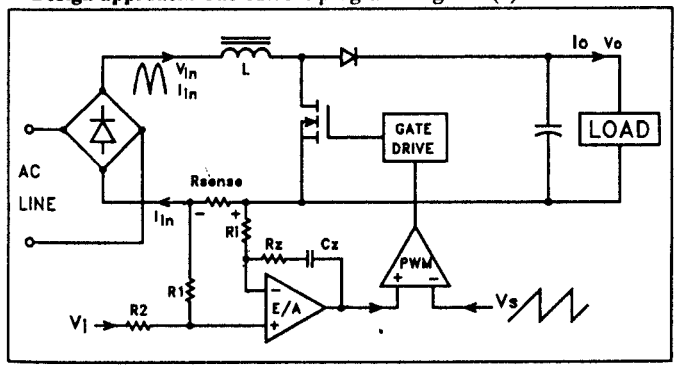


Fig. 7 - Average Current Mode Control Loop

In summary, the advantages of "average current mode control" are:

- No slope compensation required
- Good noise immunity
- No peak-avg error - inner loop actually controls "average input current" - even with flyback topology where inductor is not in input.

The one disadvantage is a somewhat reduced current loop bandwidth. This is not a problem in switching preregulator applications, considering the outer loop crossover frequency must be very low compared to the switching frequency.

(The same "average current mode control" technique can be used for multiple loop control in conventional switching voltage regulators using any power circuit topology, but at the cost of reduced current loop bandwidth.)

Sample and Hold

In a conventional switching power supply, the 0 dB loop gain crossover frequency, f_c, must be below 1/4 or 1/5 of the switching frequency, f_s. Otherwise, subharmonic oscillation occurs. This is definitely *not* a problem with a high power factor preregulator—f_c is *decades* below f_s.

In a high power factor preregulator there is a significant ripple component on the dc bus at the 120 Hz line frequency 2nd harmonic. Without sample and hold, the 120 Hz ripple passes through the control loop. This distorts the input current waveform (see Fig. 5). The amount of distortion depends on the 120 Hz loop gain. Also, if the 120 Hz loop gain is more than 1/4 - 1/5, the amplified ripple becomes so large that clipping occurs, impairing performance. Since the loop gain characteristic has a single pole rolloff (-20 dB/decade) in this region, crossover frequency f_c must be less than 1/4 - 1/5 the 120 Hz ripple frequency, or 25-30 Hz.

Additional 120 Hz ripple comes from the voltage feed-forward circuit, depending on the time constant of the averaging network. With an f_c of 20 Hz (120Hz/6) and a feed-forward time constant of 8 ms (1/2 line period), a P.F. of .95 - .98, (23% - 14% harmonic distortion) is achievable (see Table I).

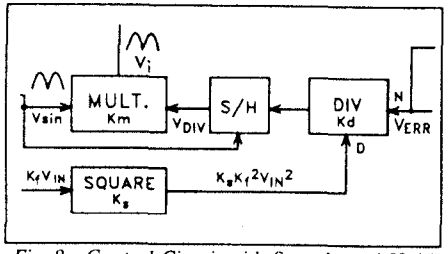


Fig. 8 - Control Circuit with Sample and Hold

If 3% input current distortion is required, f_c must be less than 120Hz/20, or 6 Hz, and the feed-forward time constant must be raised to 40 ms to reduce the harmonic levels from these sources. This *destroys* preregulator dynamics, forcing the addition of sensing/power/current limiting circuitry to override the slow loop.

As shown in Fig. 8, a sample and hold circuit placed at the control input to the multiplier is an excellent solution to this problem. The S/H samples the divider output at the very beginning of each half cycle and holds it for the entire half cycle. Thus the 120 Hz ripple from the error amplifier *and* from the feed-forward squaring circuit are eliminated. The input current programming waveform , V_i, becomes a perfect replica of V_{IN}, without distortion.

The crossover frequency is no longer limited by waveform distortion considerations, but a new limitation appears. The sampling frequency, f_{SH} (120 Hz), becomes the "switching frequency" in the small signal model of the outer loop. Also, a sampling delay is introduced in the control loop. The result is that f_c must be less than $f_{SH}/4$ to $f_{SH}/6$ or loop instability in the form of subharmonic oscillation will occur.

Also, when the sample is taken at the beginning of each half sine, the feed-forward voltage very closely approximates the average value of the input sine wave, regardless of the ripple amplitude. This means that high ripple from the feed-forward averaging network can be tolerated, and the time constant can be even shorter than 8 ms.

On the other hand, the sampling delay slows down the feed-forward response as well as the main loop. Computer simulation shows that *without* S/H and a PF of .96, slightly better dynamic response can be achieved than *with* S/H and a PF approaching 1.0.

The recommendation is: If a Power factor of .95 - .98 is acceptable, don't bother with the sample and hold. On the other hand, to achieve 3% distortion (P.F. = .999), the sample/hold technique is very useful.

Small Signal Model

The simplified small signal model of the outer voltage control loop shown in Fig. 9 is accurate at frequencies below the 120 Hz rectified line. Because the loop gain crossover frequency f_c is considerably less than 120 Hz, and decades less than the preregulator switching frequency, factors such as the rolloff of the inner current loop, the ESR zero of the bulk capacitor and the right half-plane zero of the boost topology are so much higher in frequency than f_c they are completely irrelevant to the performance of the outer loop.

The switching preregulator has the small signal output characteristic of a controlled power source, modeled as a current source shunted by a resistor. This source resistance, r, is always equal to dc load resistance R_L, so r changes when R_L changes. The control-to-output gain has a single pole, associated with the bulk filter capacitor. With a resistive load, the parallel combination of r with ac load resistance r_L ($=R_L$) results in a pole frequency $\omega_p = 2/R_L C_{DC}$. This pole frequency will usually be less than 1 or 2 Hz.

However, a load consising entirely of high efficiency switching converters is not a resistive load—it is close to being a constant power load. (Power demand is fixed and independent of the dc bus voltage as long as it is within the input range capability of the downstream converters.) A constant power load has a negative ac resistance equal to its dc load resistance, i.e., $r_L = -R_L$. The parallel combination r_s ($=R_L$) and r_L ($=-R_L$) approaches *infinity*, so the capacitor pole approaches *zero*. The resistances cancel and the model becomes simply a current source driving capacitor C_{DC}, with a slope of −1 from nearly zero frequency to well above the crossover frequency.

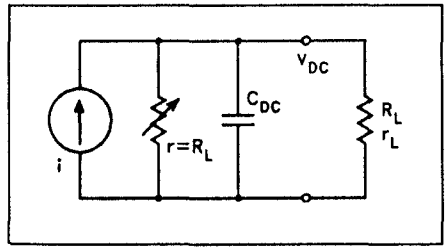


Fig. 9 - Outer Loop Small Signal Model

So r_L could be any value between $+R_L$ and $-R_L$, with the C_{DC} pole somewhere between 0 and 2 Hz. Fortunately, it really doesn't matter, and the gain in the region of interest can be expressed as:

$$v_{DC} = \frac{i_{chg}}{j\omega C_{DC}} = \frac{p_{chg}}{j\omega C_{DC} V_{DC}} \qquad (13)$$

(Note that a constant power source driving a constant power load is open-loop unstable at low frequency. The preregulator must never be tested with a negative resistance load while the voltage control loop is open—it will run away.)

The control-to-output gain also includes the modulator and ac waveshaping multiplier, as well as the feedforward divider and sample/hold, if used—everything from the error amplifier output to the dc bus preregulator output. The gain characteristic of these elements is flat with frequency, although the S/H introduces a delay of less than 1/2 line cycle, ultimately reducing the allowable crossover frequency.

Combining Eq. (13) with the small-signal version of (9) gives the control-to-output gain *without* feedforward:

$$\frac{v_{DC}}{v_{ERR}} = \frac{k_1 V_{in}^2}{j\omega C_{DC} V_{DC} R_{sense}} \qquad (14)$$

Combining Eq. (13) with the small-signal version of (10) gives the control-to-output gain *with* feedforward:

$$\frac{v_{DC}}{v_{ERR}} = \frac{k_1 k_2}{j\omega C_{DC} V_{DC} R_{sense}} \qquad (15)$$

Dimensionally, k_1 is V^{-1}, and k_2 is V^2, which resolves the dimensions of the above equations.

Because the control-to-output characteristic has a near-ideal single pole roll-off, the error amplifier gain should be flat for excellent loop stability. The gain required can be determined without a Bode plot. Simply calculate the arithmetic control-to-output gain at the desired crossover frequency using Eq. (14) at max. V_{in}, or (15) if feed-forward is used. The reciprocal of this number is the error amplifier gain required for a loop gain of 1, which is by definition the crossover frequency. The single 90° phase shift from C_{DC} assures loop stability.

A pole-zero pair could be incorporated in the error amplifier network to improve dc regulation of the dc bus voltage, but this is not recommended. There is no real advantage to

doing this because the low frequency boost cannot follow rapid line or load changes. The dc bus will have the same voltage excursions (although temporary) that would occur without this boost. In either case, the downstream converters will have to operate over the same voltage range. The only way to tighten this range is to (a) employ input voltage feedforward, and (b) increase the bulk capacitor size, which reduces the loop gain, allowing a corresponding error amplifier gain increase.

Bulk Capacitor Selection and System Performance

In any off-line supply, the input filter capacitor makes up a significant portion of the cost and the volume. Factors entering into the selection of the capacitor and the microFarads required are:

(a) ac line voltage range
(b) Power demand
(b) Holdup time (# of half cycles)
(c) Ripple voltage on dc bus
(d) Regulation of dc bus voltage
(e) Dynamics -- overshoot, undershoot
(f) ac current ratings
(g) ESR

Requirements (a) to (e) collectively determine the total dc bus voltage range the system is expected to operate under, with a variety of line and load conditions.

Conventional low power factor systems: With a full wave rectifier off the 220 V line, or voltage doubler off the 115 V line, the usual dc bus voltage range has a 2 to 1 ratio, from 200 to almost 400 V. Half of this is due to line variation, the other half due to 120 Hz ripple and holdup requirements, if any. Regulation is not possible, but this eliminates the dynamics problems often encountered with regulated systems.

The peak current charging the capacitor at the peak of each line cycle is perhaps 8 times the dc current, I_{DC}. through the dc bus. This is why the input power factor is so bad, but it also causes the rms capacitor current to be extremely high for the power input involved. With present day electrolytics, capacitors usually should be selected on the basis of their rms current rating. When this is done, the capacitance value is usually greater than the minimal size that otherwise might be used, and should provide a holdup time of one full cycle, 16 msec.

So rms current and holdup time usually dominate capacitor selection. For example with a full wave bridge rectifier, 150 μF is required with 100 W load for 20 msec holdup time to 200V from min 180V rms line. For a voltage doubler, 200 μF is needed for only 16 msec holdup time (two 400 μF in series).

High power factor systems: The $\sin^2$ charging current waveform has a peak-to-peak value only twice the dc current (Fig. 2), so the rms capacitor current is only $.707 \cdot I_{DC}$. Capacitor selection is now based primarily on holdup time, and reliability is much better because rms current is well below the rating.

With an optimized high power factor prereglator with a nominal dc bus voltage of 375 V and 100 W load, only 100 μF is required for 20 msec holdup to a minimum dc bus voltage of 320 V. Ripple is only 7 $V_{p\text{-}p}$. With voltage feedforward, the preregulator handles line voltage changes from 90 to 270 V with negligible change in dc bus voltage. Instantaneous 2:1 changes in line voltage result in overshoot and undershoot less than 5 V on the dc bus.

When the load changes instantaneously from 100 W down to 20 W, bus voltage rises from 375 to 387 V with no overshoot.

P.F. is 0.97. Loop gain at 120 Hz is -18 dB, and the crossover frequency is 15 Hz.

The above results were obtained by computer simulation, which is an excellent way to experiment with high power factor systems.

The reason that ripple is so low and holdup much better with a smaller capacitor than the low power system is very simple. The capacitor always operates with a bus voltage close to 375 V, even at low line voltage, because of the "bonus" output regulation of the high power factor preregulator. Thus the smaller capacitor consistently stores more energy than in the conventional system at low line. At higher voltage, the ΔV with a given energy withdrawn is smaller than at lower voltage.

Current Limiting with the Boost Topology

Unlike buck and flyback circuits, the boost topology cannot limit severe overcurrent because there is no series switch between input and output, only a shunt switch. High current occuring with fault load conditions and the start-up inrush current surge charging the bulk capacitor can not be limited or controlled without additional circuitry including a series switch.

Load Overcurrent Limiting: The boost topology can control and limit current only as long as the dc bus voltage, V_{DC}, is greater than v_{in}. If an overcurrent condition exceeds the preregulator power limit established by the control circuit, V_{DC} will eventually be dragged down below the peak value of the AC line voltage. When this occurs, the boost topology loses control. Current will rise rapidly and without limit through the series inductor and rectifier. Ultimately, the inductor will saturate and components will fail. The shunt switch is held *off* by the control circuit, since the current is above the desired level. It can't help to turn the switch ON -- the inductor current will rise even more rapidly and switch failure will occur.

Arguably, the downstream converters will have current limiting capability, eliminating concern about load faults. But a downstream converter or the bulk capacitor might fail. In some systems, the bulk capacitor voltage is bused to other boards or system modules, and there is a good possibility of a short circuit across this high voltage bus.

If it is considered necessary to limit the current to a safe value in the event of a downstream fault, some means external to the boost converter must be provided. This might be an additional series switching transistor or a fuse -- can it act rapidly enough??

Startup Inrush Current Limiting: Before start-up, V_o is zero. When V_{in} is switched on at the input of the boost converter, the bulk capacitor will attempt to charge resonantly to twice V_{in}. If V_{in} happens to be at the peak high-line 220 V condition (370 V) when the supply is turned on, the bulk capacitor will try to resonantly charge to 740 V. The peak resonant charging current through the inductor will be many times greater than normal full load current. To prevent saturation, the inductor must be much larger and more expensive. The boost shunt switch can do nothing to prevent this. The switch should not be turned on at all during start-up, or it will make the situation worse.

The current and voltage overshoot in the start-up scenario described above is intolerable. A fuse is no solution -- the fuse would blow each time to supply is turned on.

There are several methods that may be used to solve the start-up problem:

1. **"Start-up" bypass:** A additional rectifier bypassing the the boost inductor and rectifier diverts the start-up inrush current away from the boost inductor, as shown in Fig. 10. The bulk capacitor charges through D_{bypass} to the peak AC line voltage without resonant overshoot and without excessive inductor current. Under normal operating conditions, V_{DC} is higher than peak V_{in} , and D_{bypass} is reverse biased. If load overcurrent pulls down V_{DC}, D_{bypass} conducts, but this is probably preferable to having the boost inductor carry the overload.

Inrush current is high with this technique, limited only by line impedance, the same as a simple capacitor input filter. A resistor in series with D_{bypass} could theoretically limit the inrush, but a resistance large enough to have a significant effect passes most of the start-up inrush back to the inductor.

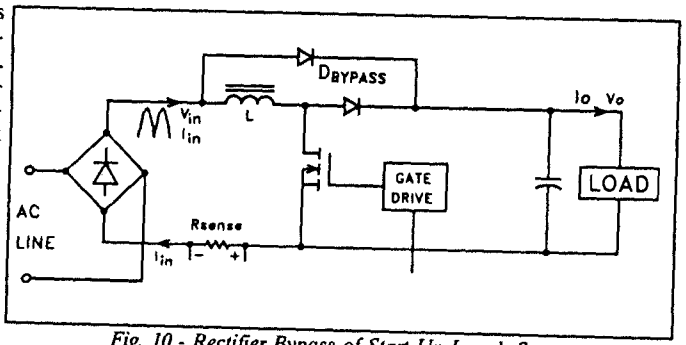


Fig. 10 - Rectifier Bypass of Start-Up Inrush Surge

2. **External inrush limiting circuit:** A thermistor in series with the preregulator input will limit the inrush current, but it has losses and is used only in low power systems. Also, the thermistor cannot respond fast enough to provide protection after a line dropout of a few cycles.

A more efficient approach uses a series input resistor shunted by a Triac or SCR which turns on toward the end of the surge, after the voltage across the inrush limiting resistor diminishes. A control circuit is necessary. This method can function on a cycle-by-cycle basis for protection after a dropout. It is frequently used at higher power levels, but its cost can be excessive for low power applications. It does not protect against load overcurrent.[2]

3. **"Buck or Boost" Topology:** Adding an additional series transistor and free-wheeling rectifier ahead of the boost inductor as shown in Fig. 11 provides a circuit which can limit load overcurrent as well as start-up inrush surge. It operates in *either* boost mode or buck mode. The series (buck) switch functions for current limiting only and has its own control circuit. Under normal conditions the buck transistor is continuously *on* and the circuit functions strictly as a boost converter. During load overcurrent or start-up surge conditions when V_{DC} is below V_{IN}, the shunt (boost) switch is kept continuously *off* by its independent control circuit and the buck switch is pulse width modulated by its overcurrent controller to limit the current to the desired level. Both controllers share the same current sense resistor.

In the buck regulator mode, input current is chopped, generating noise at the input, but this happens only under overcurrent conditions.

(This two-transistor topology can also be used, with a different control circuit, in the buck-boost (flyback) mode. This is achieved by pulse width modulating both switches in a complementary manner, with the buck switch *on* while the boost switch is *off*, and vice-versa. This is a two-transistor flyback configuration. It functions whether V_{DC} is greater or less than V_{IN} so it can be used in a high power factor preregulator supplying a 300 V bus from 220 V line, for example.)

Miscellaneous Considerations

The following considerations are pertinent in designing high power factor circuits:

Power Factor vs. harmonic content: Figure 5 shows the rectified input current waveform with 0.96 Power Factor. This rectified current waveform distortion is caused by the 120 Hz ripple on the dc bus and the 120 Hz feed-forward ripple which are both passed through the control circuit and distort the current programming waveform. As shown in Figure 5, the rectified current waveform distortion is mainly phase-shifted 120 Hz.

However, this 120 Hz *rectified* waveform distortion translates into a 90° leading 60 Hz component and a third harmonic component in the *unrectified* line current on the input side of the bridge rectifier. These two components have the same amplitude. With a Power Factor of 0.96, the 90° leading component is 20% and the 3rd harmonic distortion component is also 20% of the in-phase fundamental.

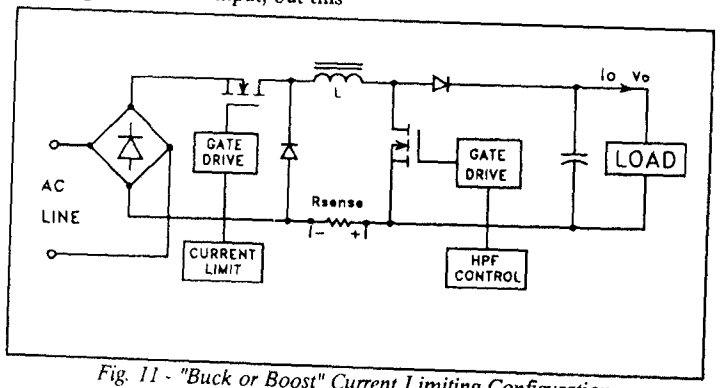


Fig. 11 - "Buck or Boost" Current Limiting Configuration

The relationship between the total rms line current with its various components and the Power Factor is:

$$I_{rms} = (I_{f0}^2 + I_{f90}^2 + I_{H3}^2)^{1/2}$$

$$P.F. = I_{f0}/I_{rms}$$

where I_{rms} = total rms current
I_{f0} = in-phase fundamental
I_{f90} = 90° phase-shifted fund.
I_{3H} = third harmonic

Table I shows Power Factor vs. I_{3H} and I_{f90} as a percentage of I_{f0}.

Table I - *Power Factor vs. Phase Shifted and Third Harmonic Components*

P.F.	$\%I_{f90}/I_{f0}$	$\%I_{3H}/I_{f0}$
0.87	40	40
0.92	30	30
0.95	23	23
0.98	14	14
0.997	5	5
0.999	3	3

Limiting and clamping: All of the control circuit elements—error amplifier, multiplier, divider, squaring circuit—have inherent limits on their output voltage swings. This results in waveform clipping and input current or power limiting, depending on where in the control circuit this occurs. Careful planning is required to use these inherent bounds properly to limit peak current and power while avoiding unintended limiting at operating extremes. Referring to Fig. 6:

The multiplier output clips peak V_i, thus limits peak I_{in}. R_{sense} and the divider at the current error amplifier input should be set up so that peak I_{in} is adequate for full load power at minimum V_{in}.

Divider k_{in} should be set so that with min. V_{in} and max. V_{DIV} (or max. V_{ERR} with no feed-forward), peak V_i is just below the multiplier output range limit.

Feed-forward divider k_f should be set in conjunction with the squaring circuit gain, k_s, so that the divider output is near its range boundaries at extremes of V_{in} and V_{ERR}.

With feed-forward, the error amplifier output limit can be used to limit maximum power input, regardless of Vin.

(Remember that with the boost topology, if an overload is severe enough to pull the output V_{DC} below v_{in}, the boost transistor remains off and current limiting no longer works, unless separate means are provided.)

Control circuit dc offsets: As the control signals propagate through the various control circuit stages, the original dc levels are frequently lost.

The intended zero point of the V_i current programming waveform is lost at the multiplier output. It must be brought into correspondence with the zero current level of the I_{in} waveform as seen across R_{sense}, or the I_{in} rectified sine wave will have its bottom clipped or elevated, resulting in distortion and reduced P.F.

DC offset through the feed-forward squaring and dividing circuits will hurt feed-forward linearity, reintroducing some loop gain and bandwidth variation with V_{in}, and perhaps interfering with input power limiting as set up at the error amplifier output.

The reference voltage at the error amplifier non-inverting input should be at the mid-range of the E/A output swing capability to minimize dc bus voltage offset error. Avoid using a capacitor in series with the E/A feedback to eliminate this offset—it will cause overshoot.

While these offsets can cause great difficulty in achieving very low harmonic distortion, they should be quite managable for P.F. up to 0.98. Watch out for temperature variations of these offsets.

Summary Comparison

High power factor preregulators provide many advantages and eliminate many of the problems compared with a simple capacitor input filter. In some systems, the reduced bulk capacitor cost and savings in the downstream converters because of the much narrower dc bus voltage range will pay for the increased cost of the preregulator.

Table II summarizes the comparison of a high power factor preregulator which can operate from 90 to 270 Volt rms line without range switching, vs. a conventional 90 to 135 V doubler and a 180 to 270 V full wave bridge.

Some aspects of the closed loop involving multipliers, dividers, and sample/hold elements do not fit into existing small signal models. Computer simulation is an ideal tool to evaluate and optimize high power factor circuits as part of the design process.

References

[1] R. D. Middlebrook, "Predicting Modulator Phase Lag in PWM Converter Feedback Loops," *Proceedings of Powercon 8*, pp. H4.1–H4.6, April 1981.

[2] R. Adair, "Incorporate Active Inrush Current Limiting to Improve Reliability and Efficiency of Power Supplies," *Unitrode Application Note U-83.*

[3] Power Electronics Group, California Institute of Technology, "Input-Current Shaped Ac-to-Dc Converters," *Final Report Prepared for NASA*, May, 1986.

[4] B. L. Wilkinson, J. Mandelcorn, "Unity Power Factor Supply," *U. S. Patent #4,677,366*, June, 1987

Table II - *Summary Comparisons*

100 WATT LOAD ON DC BUS

	115 V Doubler	220 V Bridge	High P. F. Preregulator
Line Voltage Range (Volts rms)	90 - 135 V	180 - 270	90 - 270
Bulk Filter Capacitance (μF)	2 x 400 μF	150	100
Holdup Time, milliseconds to min. V_{DC}:	16 ms 200 V	20 200	20 320
Normal dc Bus Voltage Range, V	228 - 381 V	226 - 381	360 - 390
Maximum Bus Ripple Voltage, p-p	18 V p-p	28	7
Power Factor	0.6	0.65	0.96

High Power Factor Switching Preregulator Design Optimization

Lloyd Dixon

Summary:

Design of a high power factor active preregulator is optimized to achieve less than 3% harmonic distortion and power factor better than .995 without a sample/hold. The circuit operates over a line voltage range exceeding 3:1 and at loads approaching zero. Under these wide-ranging conditions, the loop gain is constant and the dynamic response to large transient changes in line and load is excellent.

General Perspective

Off-line switching power supplies have historically used full wave rectifier bridges with simple capacitor input filters to power the DC input bus. The line current waveform is a narrow pulse resulting in notoriously poor power factor (0.5–0.6) and harmonic distortion (>100% of the fundamental). Line circuit breakers trip prematurely, and line noise causes a variety of problems.

Among the wide variety of active methods for improving power factor and harmonic distortion, the circuit of Fig. 1 is remarkably effective. An earlier version of this circuit was discussed in detail in Ref. [1].

Summarizing the operation of Fig. 1, the block labeled "High Power Factor Switching Preregulator" contains a power circuit (boost, flyback or buck) and an *input* current control circuit. The preregulator is controlled by current programming signal I_{CP} to draw input current in a nearly perfect rectified sine waveform in phase with the input voltage.

The current programming signal I_{CP} is generated by multiplying a full-wave rectified "pattern" i_{AC} derived from V_{IN} by a control level that varies inversely with output voltage deviation. This voltage control loop crudely regulates the output bus voltage.

A voltage V_{FF} proportional to rms input volts is squared and divided into the control level. This feature is essential to operation over a wide range of input and output conditions with constant loop gain and good response.

Although the circuit appears complex, all of the control functions shown in Fig. 1, including current control within the preregulator block, have been incorporated into a single integrated circuit–the UC3854 [3].

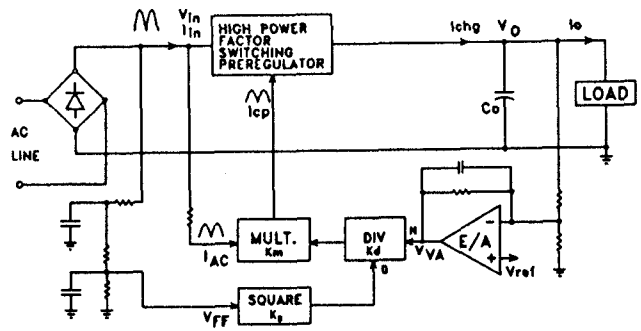


Fig. 1 - High Power Factor Preregulator

Confusion can easily occur between line frequency and switching frequency values - peak 60 Hz current is average 100kHz, peak 100kHz may be much higher than the 60 Hz peak.

To simplify the discussion, 60 Hz line frequency and 100kHz switching frequency is normally assumed.

additional 90° through the *VEA*, for a total lag of 180°. The positive peaks of the 2nd harmonic waveform now coincide with the line peaks, distorting the line current waveform by increasing its peak value and taking it toward a triangular shape. Note that the deviation between ideal and actual still has equal 3rd harmonic and fundamental components–both 5%, half the 2nd harmonic–but the fundamental component is now in phase with the line voltage waveform so it is neither distortion nor does it hurt the power factor as it did with the single-pole loop. The fundamental component increases the output power by 5%, but the voltage loop quickly adjusts the *VEA* output downward by 5% to maintain the correct power. The peak current is then only 5% higher than the ideal sine wave, due to the 3rd harmonic peak.

Using a second pole placed at f_C to achieve low distortion with excellent voltage loop bandwidth is only practical when a technique such as voltage feed-forward is used to provide constant control loop gain. Otherwise, loop gain and f_C vary with the V_{IN}^2, making placement of the second pole practically impossible.

Distortion Arising from Second Harmonics on the Feedforward Signal: The feedforward signal V_{FF} is proportional to the rms line voltage. It is obtained by averaging the rectified input voltage, as shown in Fig. 1. The rectified input voltage has a large 2nd harmonic component (66% of the average value). The 2nd harmonic is greatly attenuated through the averaging network, but some 2nd harmonic will exist with the DC feedforward signal, V_{FF}. As an example, 5% 2nd harmonic on V_{FF} is doubled through the squaring circuit to 10%. It remains at 10% through the divider and ultimately results in 5% 3rd harmonic distortion plus 5% fundamental. This process is the same as the distortion caused by 2nd harmonics through the *VEA* shown in Fig. 3 except the V_{FF} harmonics are doubled through the squarer. To summarize: *Line current % 3rd harmonic distortion equals the % 2nd harmonic on* V_{FF}.

Unfortunately, the % 2nd harmonic from V_{VEA} and V_{FF} are in phase at the input of the multiplier and effectively add together. For example, 2% harmonic on V_{FF} plus 2% on $V_{VEA}(/2)$ = 3% 3rd harmonic on the input line current.

The feedforward time constant should be short to get fast correction for sudden line voltage changes, but this increases the 2nd harmonic on V_{FF}. As single pole V_{FF} averaging network with adequate response time produces quit a bit of distortion (see Ref [1]). The 2-pole system shown in Fig. 1 is a great improvement. Fig. 4 shows the improved response of a 2-pole network compared to a 1-pole network with the same % second harmonic output.

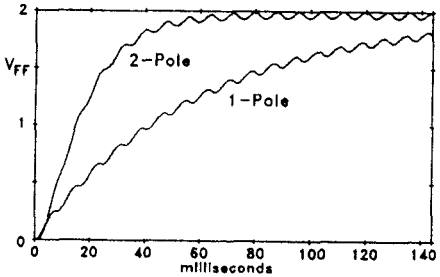


Fig. 4 -- 2-Pole vs. 1-Pole Feedforward

Other even harmonics are present on the rectified V_{IN} waveform, but they are initially much lower amplitude than the 2nd harmonic and are attenuated much more through the feedforward averaging network, so they contribute a negligible amount of input distortion. As a practical matter, only 3rd harmonic distortion is generated through the feedback and feedforward paths. Other harmonic frequencies will be generated if input current tracking is poor, however.

In Ref [1] the statement is made that 3% harmonic distortion is impossible to achieve without a technique such as a sample/hold. But with 2-pole characteristics in the feedback and feedforward paths, this statement is not correct.

Designing the Power Circuit:

Selection of the Power Circuit Topology: Historically, the boost converter operated in the continuous mode has been the most popular configuration. At least part of the reason is that the chopped input current waveforms of the flyback and buck topologies have been difficult to control adequately using peak or hysteretic CMC.

Much greater freedom of choice is possible with average CMC. Input current is directly sensed, averaged and controlled: inductor current with the boost topology, chopped switch current with flyback or buck circuits. Using average CMC, the external characteristics of the closed current loop are identical for all topologies–a flat gain characteristic with single pole roll-off at the current loop crossover frequency.

In addition, any of these topologies can cross the mode boundary and operate effectively in the discontinuous mode. This eliminates concerns regarding minimum loads. For the same reason, the inductance value can be reduced considerably, diminishing cost and weight. Minimum inductance is determined only by considerations of max. peak current in the switch and rectifier at low line voltage. At high line, the full load current might be entirely discontinuous.

With average CMC, the choice of the power circuit can be made on the basis of the application, not the control method. See p4, Ref.[1] for a discussion of the various topologies. Contrary to the statement of unsuitability made in [1], the buck regulator might be the best choice for low voltage outputs such as battery charging or 48V telephone power supplies. The buck regulator will cease functioning as the instantaneous line voltage moves below the output voltage as it approaches zero crossing. This puts a step in the input current waveform. A power factor of 0.98 is easily achievable, however, but not 3% harmonic distortion.

Designing the Boost Converter:

This analysis of a 1kW boost converter power stage shown in Fig. 5will use the following application to demonstrate the design approach:

Input Volts, V_{IN} : 80 - 270 V rms
Output Volts, V_O : 380Vdc
10% Overload Power Limit : 1100W
Switching Frequency, f_S : 100 kHz

Selecting the Inductor value: The inductor value determines the amount of switching frequency ripple that rides upon the line current sine wave. One consideration is input noise, the other is peak current through the transistor switch and rectifier. With average CMC, discontinuous operation and minimum loads are not a concern. Peak current is worst case at low line (80Vrms, 113Vpk) and full power (1000W). The max. peak 60Hz current is:

$$I_{60pk} = \frac{P_{OL}\sqrt{2}}{V_{INmin}} = \frac{1000\sqrt{2}}{80} = 17.7A \quad (1)$$

The overload peak 60 Hz current limit should be set at 18A.

The inductance value determines the 100kHz ripple. Half the peak-peak ripple is added to the peak 60 Hz current. The amount tolerable depends on how comfortable the switch and rectifier will be at the higher instantaneous peak current levels. 4A pp ripple will increase the max. peak 100kHz current to 20A, while 8A pp will take the peak current to 22A. The inductance can then be calculated at the peak low line input voltage:

$$D = \frac{V_O - V_{IN}}{V_O} = \frac{380 - 113}{380} = 0.702$$

$$L = \frac{V_{IN} D}{\Delta I f_S} = \frac{113 \times 0.7}{4 \times 100K} = 0.198\,\text{mH} \quad (2)$$

Allowing a ripple current of 8A pp would reduce L to .099 mH.

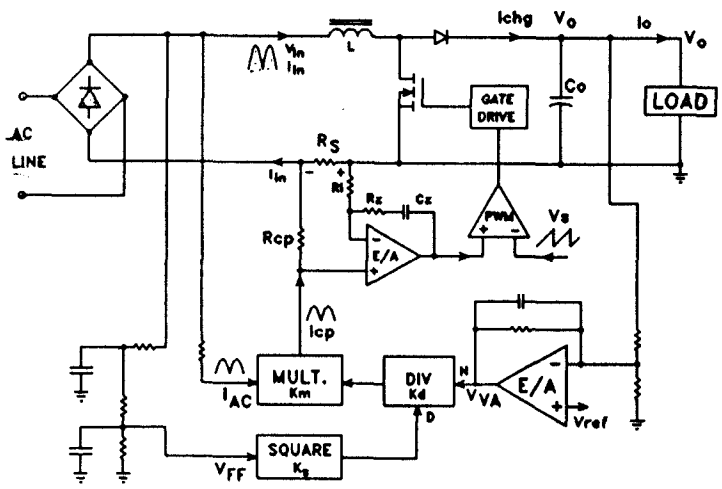


Fig. 5 - Boost Regulator Circuit

and current waveforms are in-phase sine waves. The input power is the product of these waveforms which is a $\sin^2$ function at line frequency, equivalent to (1-cos) at twice line frequency.

With high efficiency, preregulator power input equals power output to the bulk capacitor, p_{CHG}. Because V_O is essentially a DC voltage, the current waveform i_{CHG} out of the preregulator has the same shape as the power waveform, with a frequency twice the line frequency. The amplitude of the AC component of the current waveform is equal to the DC component:

$$I_{CHGpk} = P_{INavg}/V_O \qquad (3)$$

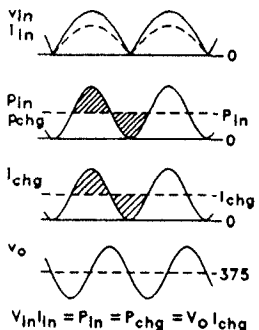
With an average power of 1kW and a 380V output bus, the DC and peak 120Hz AC charging current is 2.63A. The ripple voltage v_O across C_O is:

$$v_{Opk} = I_{CHGpk} X_C \qquad (4)$$

In practice, the bulk filter capacitance value is often determined by the holdup requirements of the supply, not by ripple voltage considerations. This means that starting from an initial bus voltage, V_O, the capacitor must store enough energy to maintain the output above a specified minimum voltage, V_{MIN}, after the line voltage has been absent for a specified number of milliseconds, often one or two full cycles at the line frequency.

$$P_O t_H = \frac{1}{2} C_O V_O^2 - \frac{1}{2} C_O V_{MIN}^2$$

Selecting the Bulk Energy Storage Capacitor Value: The output bulk filter capacitor C_O is essentially a 60 Hz filter and energy storage component (although it does filter 100kHz current as well). C_O stabilizes the output bus by storing the excess of energy provided by the line near the sine wave peaks, then providing this energy to the output when the energy available from the line is low, near zero crossing. The waveforms in Fig. 6 show the manner in which power is processed through the preregulator. NOTE: The following discussion applies to *any* properly functioning and efficient high power factor preregulator, regardless of its topology or method of current programming.



$V_{In}I_{In} = P_{In} = P_{chg} = V_O I_{chg}$

Fig. 6 - HPF Waveforms

Assuming the power factor is reasonably high, the input voltage

$$C_O = \frac{2 P_O t_H}{V_O^2 - V_{MIN}^2} \qquad (6)$$

For example, at a nominal V_O of 380V, a capacitance of 2μF/Watt will reach 353V after 20 msec, or 323V after 40 msec.

With 2μF/Watt and 380V bus, Eqs. (3) and (4) indicate an output ripple voltage v_O of 3.5Vpp (1.74Vpk). The larger the capacitance, the easier it is to achieve low distortion. With 2μF/Watt and V_O = 380V, it is not difficult to achieve 3% harmonic distortion with excellent dynamic behavior using the design approach discussed herein.

The Current Sense Resistor:

There is a great deal of flexibility in setting the value of current sense resistor R_S. If .05Ω is used to directly sense input current as shown in Fig. 5, the max peak 60 Hz current of 18A corresponds to 0.9Vpk across R_s. Power dissipation at full load, low line is 7.8W. If R_S is reduced to .01Ω, 18A peak 60 Hz equates to 0.18 volts across R_S with 1.6W dissipation. At this level, noise problems may be more severe and 4-terminal Kelvin connections may be desirable. 1 or 2% resistor accuracy is desirable throughout the current control system, otherwise tolerances may conspire to clip the current waveform at low line and full power.

For a 1kW preregulator, the best approach is probably to use current transformers (CTs) to sense the input current–see Ref [1]. In a boost preregulator, a single CT cannot be used to directly sense input (inductor) current because the DC value is lost through the CT. As discussed in [1], two CTs must be used–one senses switch current, the other senses rectifier current. The CTs reset while these discontinuous waveforms are at zero, so that the average value is retained on the secondary side. These two waveforms are applied through diodes to a common sense resistor, thereby reconstituting the input current including its average value. For example, with 200:1 turns ratio CTs (Pulse Engineering #51688 current sense inductor) a 10Ω sense resistor provides the same 0.9V with 18A max peak 60 Hz line current as the direct .05Ω current sense resistor, but the power dissipation in R_S is only 39mW. Overall preregulator efficiency is improved by almost 1%!

Setting Up the Multiplier/Divider:

The multiplier/divider must be set up so that overload power limits and independent overload current limits function properly over the entire range of input voltages and do not conflict with each other. The specifics of how to accomplish this depends on the control system used. This discussion will focus on the UC3854 control IC. Refer to Fig. 5, which shows most of the UC3854 circuitry.

The equation governing the UC3854 multiplier/divider/squarer circuits is:

$$i_{CP} = \frac{K_M i_{AC} (V_{VEA} - 1)}{V_{FF}^2} \qquad (7)$$

The power input to the preregulator is set by the error amplifier output V_{VEA}. Feedforward causes power input to remain constant at a specific V_{VEA} level regardless of line voltage changes. (Suppose line voltage doubles. I_{AC} doubles, V_{FF}^2 quadruples. i_{CP} and line current are halved, maintaining constant power input.) A very important aspect is: *The divider input in the UC3854 does not function beyond 5.6V. This V_{VEA} value corresponds to the max. overload power limit and must be set up appropriately.* It is convenient to establish 5.0V as the full load V_{VEA} value, with 5.6V for the overload power limit.

The overload power limit governs when the line voltage is in the normal operating range causing the effective current limit to vary inversely with line voltage. But with line undervoltage, or during startup or following line voltage dropout, an independent current limit is necessary. This independent peak 60Hz limit should be set at the peak 60Hz current level corresponding to full power at low line. This independent current limit is set in the UC3854 by resistor R_{SET} (not shown in Fig. 5).

Another rule that must be observed with the UC3854 is that i_{CP} cannot exceed twice i_{AC}.

There is a minimum value of V_{FF} that will satisfy this requirement at full power (V_{VEA}=5.0V). Solving Eq (7) for V_{FF} with i_{CP} set at twice i_{AC} and V_{VEA}=5V:

$$\min V_{FF} = \sqrt{\frac{K_M i_{AC}(V_{VEA}-1)}{i_{CP}}} \quad (8)$$

$$= \frac{\sqrt{1(5-1)}}{2} = 1.414\,V$$

The procedure for setting up the UC3854 multiplier is:

1. Determine the feedforward divider ratio that provides a little more than min. V_{FF} (1.414V). at low line voltage (0.9 is DC to rms form factor of rectified sine wave):

$$\max Div.\ Ratio = 0.9\times 80V/1.414 = 51{:}1$$

Referring to Fig. 5, in this example the three resistors in the divider are: 820K at the top, then 75K, with 20K at the bottom of the divider string. The divider ratio is 45.75. V_{FF} is 1.57V at 80v rms input, rising to 5.3V at 270V input.

2. The definition of i_{AC} is somewhat arbitrary. A 680K resistor from the rectified line will dissipate only 0.1W at high line. Peak i_{AC} at low line is 80•1.414/620K = .182mA pk.

3. Using values of V_{FF} and peak i_{AC} at low line, and V_{VEA}=5V at full power, use Eq. (7) to calculate the max peak current programming signal, i_{CP}:

$$\max i_{CPpk} = \frac{1\bullet.182(5-1)}{1.57^2} = 0.295\,mA \quad (9)$$

4. Finally, set the independent i_{CP} current limit to the same value found in (9):

$$R_{SET} = 3.75V/i_{CP} = 3.75/.295 = 12.7\,K \quad (10)$$

Designing the Average Current Mode Control Loop:

The maximum peak current programming value i_{CP} at full power and low line from Eq.(9) must now be equated to the actual peak 60 Hz current under these same conditions I_{60pk} from Eq.(1) -- 17.7A:

$$i_{CP}R_{CP} = I_{60pk}R_S/n \quad (11)$$

where n is the CT turns ratio, if used. Solving for R_{CP} and using the values previously established:

$$R_{CP} = \frac{17.7\,A\bullet 10\Omega/200}{0.295} = 3\,K \quad (12)$$

See Ref. [1] for the details on designing the current loop.

Once the average CMC loop is closed around the buck and flyback topologies, their characteristics appear identical to the outer voltage loop. Except for the design of the power stage, the techniques presented here apply to all topologies using average CMC.

Designing the Voltage Control Loop:

As mentioned earlier, the bulk filter capacitor size has a significant effect on the trade-off between low input harmonic distortion and acceptable excursions of the output bus voltage with rapid line or load changes. Halving C_O will double output ripple voltage and double control to output gain. If the EA gain is halved, keeping the same pole frequency, voltage loop crossover and gain bandwidth will be the same as before. Input power factor will be the same. *However* -- output bus ripple will be doubled, and output voltage transient excursions are doubled in amplitude -- perhaps to an unacceptable level. This occurs even though the overall gain-bandwidth is the same, because gain has been "relocated" -- the power circuit gain has been increased but feedback gain is decreased.

If a large C_O value is dictated by a holdup requirement of 1 or 2 line cycles, there is little difficulty achieving 3% distortion with acceptable transient behavior. but if there is no holdup requirement and the desire is to minimize C_O. some choices have to be made: 1. Keep the same f_C and gain bandwidth but have double the output ripple and transient excursions as above, or 2. Double the EA crossover and gain bandwidth which will reduce the excursions, but the ripple won't change and the harmonic distortion will double.

For this example, C_O of 2000μF (2μF/W) is assumed, providing 20ms holdup 353V min. from 380V.

The design procedure for the voltage control loop is as follows:

1. Calculate output ripple: Combining Equations (3) and (4) and solving for peak 120 Hz ripple across C_O at full power:

$$v_{Opk} = \frac{P_{INavg}X_{Co}}{V_O} \quad (13)$$

$$v_{Opk} = \frac{1000}{2\pi\,120\bullet 2000\times 10^{-6}\bullet 380} = 1.75\,V_{pk}$$

or 3.75Vpp.

2. Decide how much input current distortion will be contributed by the feedback path and the related 2nd harmonic ripple on the VEA output. To keep input 3rd harmonic distortion under 3%, the contribution from the feedback voltage will be limited to 0.75%. (Another 1.5% will be contributed by voltage feedforward, leaving a margin of 0.75% for other sources of input distortion.) The 0.75% 3rd harmonic contribution is generated by 1.5% second harmonic distortion on the *VEA* output. This means that the peak 120 Hz ripple on the *VEA* output at full load will be 1.5% of the effective V_{VEA} DC level (5V-1V):

$$v_{VEApk} = \%Ripple\times V_{VEA} = .015(5-1) = .06\,V \quad (15)$$

3. From the results of steps 1 and 2 above, calculate VEA gain desired at 120 Hz: (16)

$$G_{VEA} = v_{VEApk}/v_{Opk} = .06/1.745 = .034$$

4. Select the VEA input resistor value: Referring to Fig. 7, this is a somewhat arbitrary decision. Op amp bias current will cause errors if R_I is too large, and a small resistor will have high power dissipation. An R_I value of 1 megΩ will dissipate only 0.144 W.

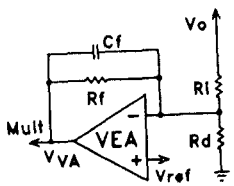


Fig. 7 - Voltage E/A

5. Calculate C_F value: C_F together with R_I determine the VEA gain, which varies inversely with frequency. C_F is calculated to achieve the desired gain at 120 Hz from step 3. *Divider resistor R_D has absolutely no effect on the error amplifier gain at any frequency. The VEA inverting input voltage is constant -- equal to V_{REF} on the non-inverting input -- so there is absolutely no AC current through R_D.*

$$C_F = \frac{1}{2\pi\,2f_L G_{VEA} R_I} \quad (17)$$

$$C_F = \frac{1}{2\pi\,120\bullet .035\bullet 1\times 10^6} = .038\mu F$$

.036μF will be used.

6. Calculate and plot the VEA gain and power circuit gain:

$$G_{VEA} = \frac{v_{VEA}}{v_O} = \frac{-jX_{Cf}}{R_I} = \frac{-j}{2\pi f R_I C_F} \quad (19)$$

$$G_{VEA} = \frac{-j}{2\pi f .036\bullet 1} = -j4.4/f$$

Power circuit gain includes the multiplier gain. The relationship between P_{IN} and V_{VEA} is linear, so the AC and DC ratio is the same. The following equation applies to *any* topology using average CMC:

$$G_{PWR} = \frac{v_O}{v_{VEA}} = \frac{P_{IN}}{\Delta V_{VEA}}\frac{-jX_{Co}}{V_O} \quad (21)$$

$$G_{PWR} = \frac{1000}{(5-1)} \frac{-j}{2\pi f 2000\times10^{-6}\cdot 380} = -j53/f$$

The two gain slopes previously calculated are now plotted in the Bode plot of Fig. 8.

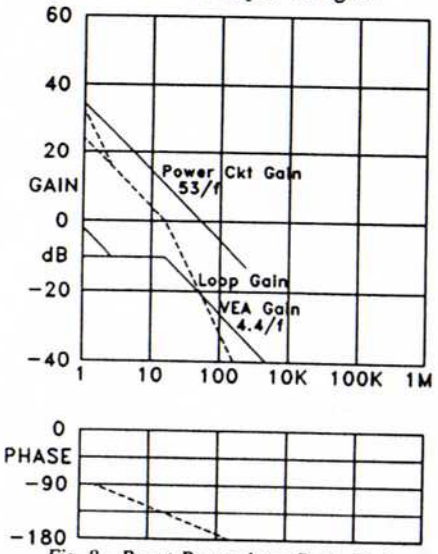


Fig. 8 - Boost Preregulator Bode Plot

The power circuit dB gain and the *VEA* dB gain can be added together on the logarithmic Bode plot to obtain the overall loop gain plot. The overall gain has a −2 slope at the crossover frequency f_C and will be unstable unless a pole is added near f_C. Fig. 8 shows the pole added to the *VEA* gain right at f_C. Below f_C, the VEA gain is flat and the overall loop gain has a -1 slope. This provides a 45° phase margin for optimum loop response.

Calculate the loop gain crossover frequency: The crossover frequency can be determined graphically from the Bode plot, but it is easier in this case to calculate it. Multiply the power circuit and *VEA* gain equations to obtain the overall loop gain, and set the result to zero:

$$G_{PWR}\cdot G_{VEA} = \frac{53}{f}\frac{4.4}{f} = \frac{233}{f^2} = 1 \quad (23)$$

$$f_C = \sqrt{233} = 15.3\,\text{Hz}$$

7. Calculate R_F to put a pole at f_C:

$$R_F = \frac{1}{2\pi f_C \cdot C_F} \quad (25)$$

$$R_F = \frac{1}{2\pi\, 15.3\cdot.036\times10^{-6}} = 290\text{K}$$

8. Calculate the divider resistor value R_D to set V_O at 380V: In the error amplifier circuit as shown in Fig. 7, there is a DC current through R_F that complicates setting up the divider ratio. The alternative is to put a capacitor in series with R_F (not shown) which eliminates the DC error and adds a zero to the *VEA* compensation network. This is not as good as it sounds, in this application. The zero frequency should be at or below 1/6 of the previously established pole frequency, or there will not be enough phase margin at f_C. This requires a capacitor 5 times bigger than C_F (not 6 times bigger). This large capacitor will charge to "wrong" voltage levels when the VEA is overdriven during startup and line voltage dropouts, and this will delay recovery. With the capacitor in series with R_F, although DC load regulation of the output is better, the peak-to-peak plus and minus transient excursions on the output bus when the load increases and decreases suddenly are twice the voltage range that will occur without the series capacitor. Try it!

In the *VEA* circuit as shown, calculate the error offset current through R_F, assuming that V_{VEA} is at 3V, the middle of its 1V-5V normal range:

$$I_{RF} = \frac{7.5V-3V}{R_F} = 15\,\mu A$$

Calculate the current through R_I:

$$I_{RI} = \frac{380-7.5}{1M} = 372\,\mu A$$

The current through R_D is:

$$I_{RD} = 372-15 = 357\,\mu A$$

Finally, calculate R_D:

$$R_D = \frac{7.5}{357} = 21K$$

It is worth mentioning again that with voltage feedforward applied as with the UC3854, the *VEA* output level programs a specific input power level, regardless of V_{IN}. As V_{EA} increases, power input increases until 5.6V is reached—the UC3854 multiplier/divider input functional limit. This 5.6V V_{EA} should be set to correspond to the overload power limit. During startup or immediately after a line dropout, the feedforward voltage V_{FF} delay would cause excessive power demand, so it is necessary to have an independent 60Hz peak current limit. This is established in the UC1854 with resistor R_{SET}. The UC1854 also provides an instantaneous peak current limit.

In the UC1854, the VEA output is limited to +16V, which means that under startup or line dropout conditions, V_{VEA} will proceed well past the 5.6V power limit level. The feedback capacitor C_F will charge to this level, delaying subsequent recovery. It is a good idea to clamp the *VEA* output (VAOUT, Pin 7), through a diode to the 7.5V reference to prevent this.

Designing the Feedforward Circuit:

The voltage divider for the feedforward network was defined in Step 1 of the multiplier/divider setup procedure. The resistor values are shown in Fig. 9.

The % 2nd harmonic present in a full wave rectified waveform is 66.2% of the DC average value. With no capacitors in the feedforward network, the % 2nd harmonic on V_{FF} is exactly the same, If it is desired that the feedforward circuit contribute only 1.5% 3rd harmonic distortion to the input waveform (leaving room for other sources of distortion), then the % 2nd harmonic on V_{FF} must be reduced to 1.5%. The attenuation factor is therefore 1.5%/66.2% or .0226. Although not recommended, a single pole may be used to achieve this reduction by placing a single 3μF capacitor across the 20K divider resistor. The resulting pole frequency of 2.7 Hz results in an attenuation factor of 2.7/120 = .0225 to achieve the desired result. But the feedforward transient response is slowed so much that unacceptable dynamic behavior results. The desired 2nd harmonic attenuation can be obtained with acceptable transient behavior by using two cascaded poles instead of one. Each of the cascaded poles should provide an attenuation factor equal to the square root of .0226, or an attenuation factor of 0.15. The required pole frequencies are 0.15•120 Hz, or 18 Hz. This is achieved using 0.5μF and 0.1μF capacitors as shown in Fig. 9. Refer back to Fig. 4 to see the improvement in feedforward response that results. Fig. 10 shows the excellent transient behavior achieved with this fast feedforward network. The line voltage was changed instantaneously from 180V rms to 270V and back again -- the entire min to max range of a 220V line.

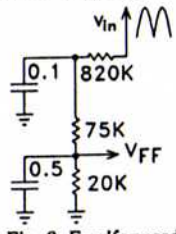


Fig. 9 Feedforward

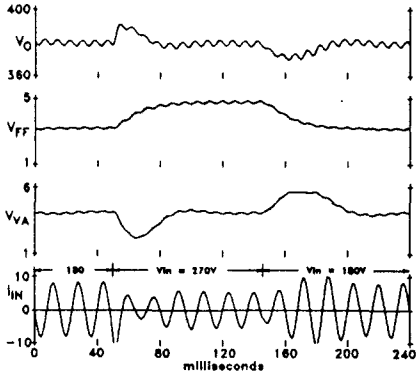


Fig. 10 - Line Regulation Waveforms

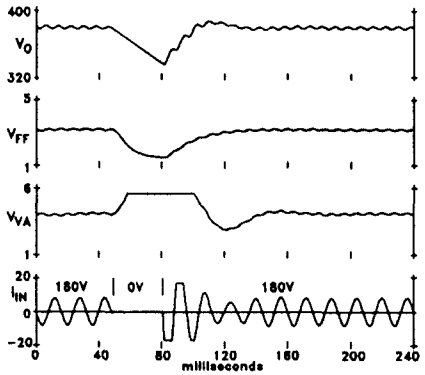


Fig. 11 - 32 millisecond Line Dropout

Line Voltage Dropouts: Fig. 11 shows that the UC3854 is quick and effective in regaining control after a line voltage dropout of 32 msec–two complete line cycles at 60 Hz. The circuit is operating at 1000W full load with 180V rms input before the dropout occurs at 48 msec on the time scale. The linear drop in output voltage is unavoidable–the output capacitor discharges into the 1000W load with no replenishment possible. Feedforward voltage V_{FF} diminishes, and the voltage error amplifier output V_{VEA} reaches the maximum multiplier input voltage, calling vainly for maximum power.

When the line voltage reappears at 80 msec, with V_{VEA} high the multiplier calls for full power. But V_{FF} cannot rise instantaneously, so the multiplier is mislead into calling for high current, restricted only by the 18A peak current limit. High power recharges the capacitor in a few half cycles, with a few volts of overshoot in V_O because of the slight delay in V_{VEA}.

The feedforward network will recover more rapidly after a line voltage dropout if V_{FF} is prevented from dropping all the way to zero. This may be accomplished by clamping the juncture of the 820K and 75K resistors to the 7.5V reference. V_{FF} will be supported at 1.47V, below the normal minimum of 1.57V.

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MAGNETICS DEFINITIONS AND EQUATIONS

SYMBOLS, UNITS, AND CONVERSION FACTORS:

Parameter	Symbol	SI Units	CGS Units	CGS to SI
Magnetic Flux Density	B	Tesla	Gauss	10^{-4}
Magnetic Field Intensity	H	A-T/m	Oersted	$1000/4\pi$
Permeability (Free Space)	μ_o	$4\pi \cdot 10^{-7}$	1	$4\pi \cdot 10^{-7}$
Permeability (Relative)	μ_r			1
Effective Magnetic Area	A_e	m^2	cm^2	10^{-4}
Mean Magnetic Path Length	ℓ_e	m	cm	10^{-2}
Air Gap Length	ℓ_g	m	cm	10^{-2}
Magnetic Flux ($\int BdA$)	Φ	Weber	Maxwell	10^{-8}
Magnetic Potential ($\int Hdl$)	mmf	Amp-Turn	Gilbert	$10/4\pi$
Inductance	L	Henry	*Henry	1
Inductance Index	AL	nH (1turn)	nH (1turn)	1
Window Area of Core	A_w	m^2	cm^2	10^{-4}
Wire Cross Section Area	A_x	m^2	cm^2	10^{-4}
Number of turns	N			1
Mean Length per Turn	l_t	m	cm	10^{-2}
Current Density	J	A/m^2	A/cm^2	10^4
Resistivity	ρ	Ω-m	Ω-cm	10^{-2}
Area Product, A_wA_e	AP	m^4	cm^4	10^{-8}
Energy	W	Joule	Erg	10^{-7}

*Commonly used in place of Abhenrys = Henries.10^9.

BASIC EQUATIONS AND DERIVATIONS (SI Units):

International standard (SI) units (rationalized MKS) are used in the following derivations. The equations are often dimensionally modified in application to allow the use of centimeters instead of meters.

Assumptions used (within the region of interest):

1. Uniform distribution of Flux Density, B
2. Uniform distribution of Field Intensity, H
3. Constant Permeability, μ_r (Linear B/H characteristic)

Magnetic Field Relationship:

$$B = \mu_o \mu_r H \qquad (1)$$

Magnetic Potential, from Ampere's Law:

$$mmf = \int H\, d\ell = H\ell = NI \quad \text{Ampere-Turns} \qquad (2)$$

Faraday's Law of Induction:

$$E = N\frac{d\Phi}{dt} = N A_e \frac{dB}{dt} \quad \text{Volts} \qquad (3)$$

Switching Power Supply Control Loop Design

Lloyd Dixon

Summary:

This paper surveys many practical aspects of control circuit design. Topics include: different approaches for achieving Nyquist stability criteria, transient response vs. phase margin, low frequency accuracy vs. the shape of the Bode plot, why it is dangerous to depend on conditional stability, achieving the maximum crossover frequency of a switched loop., other factors which may limit loop bandwidth, sources of error, and where to place the gain needed for correction.

Other practical aspects include large signal behavior and how to minimize offset error delays of compensation capacitors in the feedback path.

Control Loop Basics

The control loop in a high performance switching power supply requires high gain, to achieve good regulation, and high bandwidth, to achieve rapid response to sudden changes of line or load.

Control loop gain inevitably declines at high frequency, limiting bandwidth. The frequency at which the loop gain crosses through 1 (0dB) is defined as the crossover frequency, *fc*. The declining loop gain at high frequency is accompanied by phase lag (in addition to the normal 180° phase shift associated with negative feedback). The amount of additional phase lag is a function of how rapidly the gain drops with frequency. According to Nyquist' stability criteria, *the loop will be unstable if the additional phase lag exceeds 180° at the crossover frequency.*

If the excess phase lag at *fc* is very close to the 180° limit, the loop will be stable but the transient response will exhibit under-damped oscillations (ringing). A clean transient response requires considerably less than 180° excess phase lag at *fc*. The amount less than 180° is referred to as *phase margin*. Thus a phase lag of 117° at *fc* corresponds to a 63° phase margin.

Fig. 1 shows the gain - phase plots of two average current mode control loops and their transient response to a step change in load current. Both loops cross over at 10 kHz.

Bode plots are simplified gain - phase plots that are convenient for depicting the frequency characteristics of a feedback loop.

The 1 POLE loop has one active pole from 10Hz to over 100kHz. Thus the phase lag at *fc* is 90° and the phase margin is also 90°. Note that with the –1 slope associated with a single pole, the gain does not rise rapidly at lower frequencies. The lower

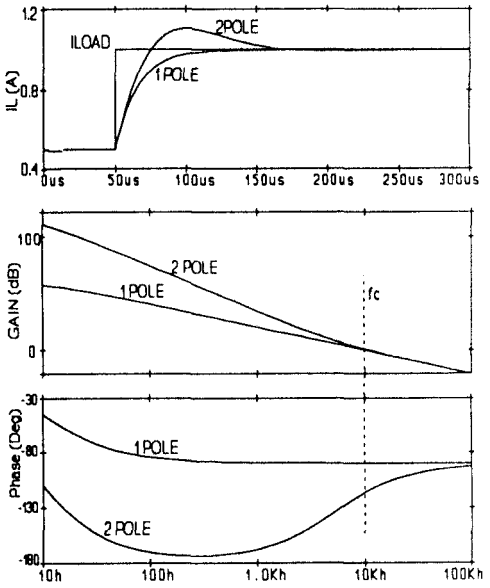

Fig. 1 - Gain - Phase Plot and Transient Response

gain/bandwidth will hurt power supply characteristics such as regulation and audio susceptibility. Note also that the transient response is slower. The area between the *ILOAD* step change and the 1 POLE response curve represents a charge deficit in the output capacitor that is never made up, except by the output voltage ultimately sagging and calling for more current.

In the 2 POLE loop, if the two poles were active through and well above *fc* (10kHz), the phase lag at *fc* would approach 180°—almost zero phase margin. The transient response would exhibit severe ringing. But the 2 poles are not active above 5kHz. A zero in the control amplifier causes a −2 to −1 slope transition at *fc*/2. This results in 117° phase lag, or a phase margin of 63°. Below 5kHz (*fc*/2), the −2 slope causes the gain to rise rapidly at lower frequencies, optimizing gain-bandwidth. With the −1/−2 zero transition at *fc*/2, transient response is critically damped—see Figure 1. The initial charge deficit is not only smaller, the slight overshoot compensates precisely for the initial deficit. This is characteristic of a critically damped system.

At frequencies well below the zero at *fc*/2, phase lag does approach 180°, and the phase margin vanishes. This is *desirable* because it is associated with the −2 slope which rises rapidly at lower frequencies, improving gain-bandwidth. 180° phase lag is also *acceptable*. Adequate phase margin is required only at *fc*. The circuit will not misbehave with 180° phase lag at frequencies *below fc*, as long as there is adequate phase margin *at fc*.

Two poles are shown occurring near 10Hz: the power circuit inductance with its series resistance, and the control circuit operational amplifier reaching its gain limit. Loop gain flattens out, and excess phase lag diminishes toward 0°.

Conditional Stability: The criteria for loop stability permits the phase shift to actually *exceed* 180° (negative phase margin) at frequencies below *fc*. This is called "conditional" stability because it depends upon the strict requirement that the phase shift be 180° (preferably much less) at the unity gain crossover frequency. Thus, the 180° limitation applies *only* at *fc* where the gain is 1, not at any lower frequency even though the gain may be high.

It is usually not wise to depend upon conditional stability. Under conditions such as startup or large rapid load changes, operational amplifiers in the loop may be driven "into the stops". This is equivalent to a temporary reduction in loop gain and crossover frequency. If phase shift exceeds 180° at the temporarily lower *fc*, the circuit will likely commence a large signal oscillation from which it cannot recover.

In summary, the gain characteristic should have a −1 (1 pole) slope as it traverses the unity gain crossover frequency. A zero at *fc*/2 will result in a −2 (2 pole) slope at lower frequencies. This will provide optimum bandwidth and critically damped transient response. The phase lag approaches 180° at lower frequencies, but this is quite acceptable. However, it is unwise to go beyond 180° and depend on conditional stability.

With inadequate phase margin, the ringing frequency will be at or near *fc*.

Crossover frequency: The unity gain crossover frequency, *fc*, is usually the best starting point for optimum control loop design, working back toward lower frequencies to obtain the best possible gain-bandwidth.

Theoretically, *fc* of a *linear* closed loop system could be at any frequency, provided the criteria for adequate phase margin are fulfilled. In practice, it becomes necessary to cross over the linear system when cumulative phase shifts of various loop components become too great to compensate. This problem is compounded when gain and phase shift of various loop elements change, sometimes unpredictably, due to tolerances and temperature effects.

Switching power supplies control loops have additional complications that can limit *fc*. The right half-plane zero encountered in the output of continuous mode boost and flyback topologies is not only near-impossible to compensate, it moves in frequency as a function of load. With voltage mode control, loop gain varies as a function of input voltage. With discontinuous operation or with current mode control, voltage loop gain varies with load. All of this can make it extremely difficult to achieve a high *fc* while adhering to Nyquist' stability criteria under all conditions of operation.

One reason current mode control can provide better control loop performance is that the current loop and the outer voltage control loop are both simplified, making it much easier to achieve high crossover frequency in both loops. For example, in a buck-derived regulator, the current loop has to deal only with the inductor pole, while the output loop deals only with the output capacitor and its variable ESR zero.

Slope limitations: Buck derived topologies are relatively easy to compensate, especially if current mode control is used. A high *fc* could be realized under Nyquist' criteria alone, but another limitation is encountered that is unique to switched loops: After the waveforms applied to the PWM comparator inputs converge, (causing the power switch to turn off), the waveforms should then *cross over* and diverge (or at a *minimum* coincide). Otherwise, subharmonic oscillation will occur under certain operating conditions. With peak current mode control, slope compensation corrects this problem (and reduces the loop gain). This problem exists in *any* switched loop, but it is more likely to be the limiting factor in buck-derived circuits. The solution requires limiting the control amplifier gain at the switching frequency, which indirectly limits *fc* to 1/3 to 1/10 of *fs*.

Other phase margin considerations: The most usual method of assuring adequate phase margin and clean transient response with minimum loss of gain-bandwidth is to put a control amplifier zero at *fc*/2, making a loop gain slope transition from −2 below *fc*/2 to −1 above. To attenuate switching noise, a control amplifier pole is sometimes added at a frequency above *fc*. This pole converts the −1 slope at *fc* to a −2 slope at higher frequencies. It should be 1 decade above the previously placed zero, and also above 2·*fc*, to maintain adequate phase margin. (Be careful—this high frequency pole may impair response for peak current limiting.)

A completely unique situation arises in the voltage loop of a high power factor preregulator. The loop gain must be very low at 2·*fLINE* (120Hz) to minimize 2nd harmonic distortion feedback. The crossover frequency, although well below *fLINE*, must be as high as possible to obtain reasonable loop dynamics. The optimum solution is to use a −2 slope *above fc* up to 2·*fLINE*, with a pole slightly above *fc* to transition to a −1 slope *below fc*.

Control Loop Design Examples

Definitions:

Rt: "transresistance"—the translation of inductor current to a voltage, v_i. In its simplest form, *Rt* = current sense resistor *Rs*. With a current transformer, *Rt* = *Rs*/*N*.

Vs Sawtooth voltage, peak-peak

fs Switching frequency

fci Current loop crossover frequency

fcv Voltage loop crossover frequency

Average Current Mode Control Loop

Fig. 2 is the circuit diagram of a buck regulator with an average current mode control loop. Fig. 3 is the small signal equivalent circuit. Fig. 4 is the Bode gain plot of the PWM/power circuit, the current amplifier, and the overall current loop gain.

Conditions:

Vi = 7-14V	*Vo* = 5V	*L* = 10µH
C = 5000µF	*Rc* = .02	*Io* = 15 → 20A
Rt = .05Ω	*Vs* = 5V	*fs* = 100kHz

Description: Referring to Fig. 2, Inductor current I_L is sensed and converted into equivalent voltage v_i by transresistance *Rt*. Current amplifier (CA) amplifies the differential between v_i and current programming voltage *VSET*. The amplified error applied to the PWM comparator controls the duty cycle of the power switch. This in turn controls the average inductor input voltage, changing current until v_i equals *VSET*. I_L then equals *VSET*/*Rt*.

Goal: Obtain the highest crossover frequency, fci, consistent with equal slopes at the PWM comparator inputs during the OFF time, and with a single active pole (-1 slope) at crossover.

Strategy: The PWM/power section has a 1-pole slope above resonance (from the filter inductor). For the overall −1 slope required at crossover, the CA gain must be flat from below *fci* to above *fs*. A zero in the CA makes the transition from −1 to −2 slope below *fci*/2 to achieve low frequency boost, with critically damped transient response.

Implementation:

Sawtooth slope:

$$dv_S/dt = Vs/Ts = 5V/10\mu sec = 0.5V/\mu sec$$

Inductor current downslope (during OFF time), converted into an equivalent voltage downslope by transimpedance *Rt*:

$$di/dt = Vo/L = 5V/10\mu H = 0.5A/\mu sec$$

$$dv_i/dt = Rt\, di/dt = .05\times 0.5 = .025V/\mu sec$$

Current Amplifier gain for equal slopes at the PWM comparator input:

$$G_{CA} = \frac{v_{CA}}{v_i} = \frac{0.5}{.025} = 20$$

Back off gain by 25% to allow for additional downslope from ESR voltage waveform passed through voltage amplifier. Use $G_{CA} = 15$:

$$Rii = 5k,\ Rfi = 75k$$

Current loop PWM/power section gain (at frequencies above *L-C* series resonance at 712Hz):

$$i_L = \frac{Vin\, d}{\omega L};\quad v_i = Vin\, d\frac{Rt}{\omega L};\quad d = \frac{v_{CA}}{Vs}$$

$$G_P = v_i/v_{CA} = \frac{Vin}{Vs}\,\frac{Rt}{\omega L} = \frac{-j159\,Vin}{fs}$$

Overall current loop gain:

$$G_I = \frac{159\,Vin}{f}\cdot 15 = \frac{2385\,Vin}{f}$$

Set Gain = 1 and *Vin*=7V to find *fci* min.:

$$fci = 2385\,Vin = 16.7\text{kHz min at } Vin=7V$$

Current Amp. compensation: Zero at *fci*/2 (8kHz)

$$Cfi = \frac{1}{2\pi f Rfi} = \frac{1}{6.28\cdot 8kHz\cdot 75k} = 260pF$$

When the current loop is closed, its gain is a transconductance: $i_L/VSET = 1/Rt$. The closed loop gain is flat until it rolls off at the open loop crossover frequency, *fci*. This characteristic makes it easy to include in the outer voltage loop.

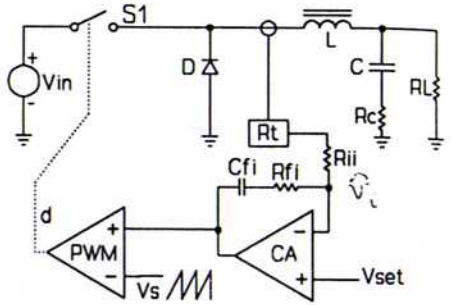

Fig. 2 - Average Current Mode Current Loop

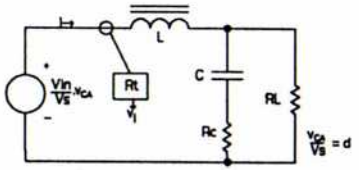

Fig. 3 - Current Loop Small Signal Equiv. Ckt

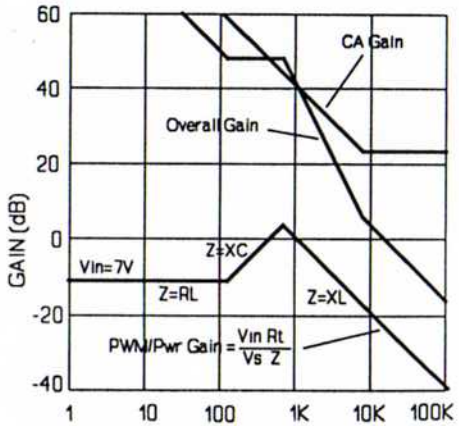

Fig. 4 - Current Loop Bode Plot

Demonstration: Fig. 5 shows the stability and transient response of the current loop with compensation as calculated above. The bottom two curves are the current programming voltage, *VSET*, and v_i, which equals $I_L \times Rt$. The top two curves are the two PWM comparator inputs: sawtooth voltage *Vs*, and the current amplifier output, v_{CA}.

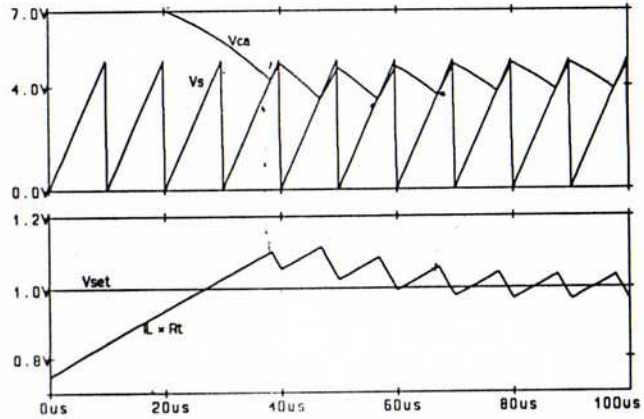

Fig. 5 - Current Loop Waveforms with Current Change

At the beginning of the demonstration, I_L has been regulating at 15A (0.75V across *Rt*). At time 0, *VSET* changes instantaneously from 0.75V to 1V. This new demand for 20A cannot possibly be fulfilled by any control circuit action. The CA output is driven to its 7V limit, calling for the power switch to be fully ON. But it takes 25μsec (several switching periods) for I_L to reach 20A at its max. slew rate of $(Vin-Vo)/L$ = 0.2A/μsec. The control loop is temporarily open.

While I_L is slewing from 15A to 20A, the error input to the CA causes feedback capacitor *Cfi* to charge, developing a voltage offset. When I_L reaches 20A, the *Cfi* offset holds the CA output out of the normal PWM input range (see Fig. 5). Thus I_L rises above 20A until the *Cfi* offset is discharged back to normal. This is not an operational flaw—it is actually beneficial. During the initial 25μsec while I_L is low, the output filter capacitor has a charge deficit. The *excess* current after 25μsec rapidly *restores this charge deficit*. If this overshoot did not occur, Vout would sag. The charge deficit would then be restored over a longer time by action of the voltage loop in an actual power supply. The overshoot results in better performance. Note that this is *not* the same as the overshoot associated with critical damping of the current loop. The current loop is in fact open during this time—this is a large signal phenomenon.

Adding the Voltage Loop

Fig. 6 is the circuit diagram of a buck regulator with a voltage control loop added to the average current mode control loop previously discussed. Fig. 7 is the voltage loop small signal equivalent circuit. Fig. 8 is the Bode gain plot of the power circuit (including the closed current loop), the voltage amplifier, and the overall voltage loop gain.

Conditions:

$Vi = 7 \rightarrow 14V$	$Vo = 5V$	$L = 10\mu H$
$C = 5000\mu F$	$Rc = .01-.02$	$Io = 15 \rightarrow 20A$
$Rt = .05\Omega$	$Vs = 5V$	$fs = 100kHz$

Description: Referring to Fig. 6, a voltage error amplifier (VA) replaces *VSET* in Fig. 2. The VA amplifies the error between *Vo* and the 5V reference. The VA output, v_{VA}, programs a constant inductor current according to the transconductance $1/Rt$ of the closed current loop.

Goal: Obtain the highest crossover frequency, *fcv*, consistent with equal slopes at the PWM comparator inputs during the OFF time, and with a single active pole (-1 slope) at crossover.

Strategy: Referring to Fig. 8, the power circuit gain equals the current loop transconductance $1/Rt$ times output impedance *Zo* which varies with

frequency. Current loop transconductance is flat up to *fci* (16.7kHz), where it rolls off with a –1 slope.

The biggest problem is with variation of *Rc*, the output capacitor ESR, and the zero it places in the loop. In this example it is assumed that *Rc* varies within a 2:1 range (.01 to .02Ω). The zero, f_{ESR} ranges between 1.6 and 3.2kHz, which is below the desired crossover frequency, *fcv*. The power circuit gain is flat from f_{ESR} through *fcv* up to min *fci*, the current loop gain roll-off at 16.7kHz.

The VA gain is made flat at switching frequency *fs*. Inductor ripple current flowing through ESR *Rc* generates a sawtooth waveform which is amplified and inverted by the VA and applied to the CA non-inverting input. This sawtooth is *in phase* with the sawtooth across *Rt* at the other CA input. Thus the OFF-time slope at the PWM comparator input is worsened. An allowance was made for this in the CA gain, but the VA output slope must be limited to 1/2 the slope across *Rt*, limiting VA gain at *fs*.

The VA gain has a zero at *fci* (16.7kHz), below which it has a –1 slope. Thus the overall voltage loop gain has a –1 slope from *fc* down to f_{ESR}. Crossover *fcv* varies with Rc from 4 to 8kHz. Below f_{ESR}, the overall voltage loop gain has a –2 slope. This boosts the voltage loop gain at lower frequencies, but also makes it important that max f_{ESR} is below minimum *fcv*.

There are two other alternatives:

1. Wide ESR zero range. If max f_{ESR} is closer to min *fci* than the above example, it will be impossible to safely cross over anywhere above f_{ESR}. VA gain must be very low and flat from well below f_{ESR} all the way up to *fs*. Overall gain rises only as the power circuit gain rises below min f_{ESR}, resulting in *fcv* way below min f_{ESR}. This is a most undesirable situation.

2. Min ESR zero above desired *fcv*. (this might be the case with ceramic output filter capacitors.) The power circuit gain has a –1 slope from the $R_L C$ pole (127Hz) all the way up to *fci*. The VA gain must be flat above *fcv*/2, and is limited by slope considerations. A zero in the VA gain gives the overall gain a –2 slope below *fcv*/2. This desirable situation can be created with electrolytic output filter capacitors by using a much higher voltage rating than necessary. (For the same size and cost, the higher voltage capacitor has the same ESR but lower capacitance, thus higher ESR zero frequency.) The penalty is a lower output surge impedance less capable of standing up to a large signal incident such as a sudden large load change.

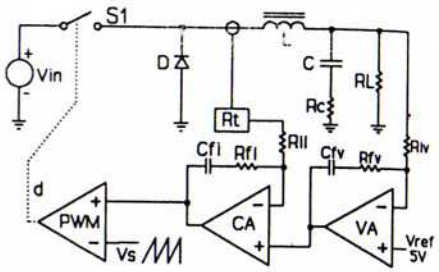

Fig. 6 - Average Current Mode Voltage Loop

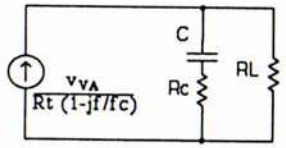

Fig. 7 - Voltage Loop Small Signal Equiv. Ckt

Implementation:

Inductor current downslope (during OFF time), converted into an equivalent voltage downslope by *Rc*, the output capacitor ESR:

$$di/dt = Vo/L = 5V/10\mu H = 0.5A/\mu sec$$

$$dv_v/dt = ESR\ di/dt = .02 \times 0.5 = .01V/\mu sec$$

Because of slope limitations at the PWM comparator, the sawtooth slope at the VA output must be limited to 1/2 the slope across *Rt* (*dvi/dt*). Thus the voltage amplifier gain at *fs* is:

$$G_{VA} = \frac{v_{VA}}{v_O} = \frac{dvi/dt}{2\,dvv/dt} = \frac{.05}{2 \times .02} = 1.2$$

$$Riv = 10k,\ Rfv = 12k$$

A zero is put in the VA gain where current loop transconductance rolls off at min *fci* (16.7kHz):

$$Cfv = \frac{1}{2\pi f_{ZERO} Rfv} = \frac{1}{6.28 \cdot 16.7kHz \cdot 12k} = 800pF$$

The VA gain below this zero is:

$$G_{VA} = \frac{v_{VA}}{v_O} = \frac{-j1.2 f_{ZERO}}{f} = \frac{-j20{,}000}{f}$$

The power circuit gain between the *ESR* zero frequency and fci (16.7kHz) is:

$$\frac{v_O}{v_{VA}} = \frac{Rc}{Rf} = \frac{.02}{.05} = 0.4$$

Overall voltage loop gain, and crossover freq., *fcv*:

$$G_V = \frac{20{,}000}{f} \cdot 0.4 = \frac{8000}{f}; \quad fcv = 8kHz$$

Demonstration: Fig. 9 shows the stability and transient response of the voltage loop. The bottom two curves are the voltage eror amplifier output, v_{VA}, and v_i, which equals $I_L \times Rt$. The top two curves are the two PWM comparator inputs: sawtooth voltage Vs, and the current amplifier output, v_{CA}. The output voltage is not shown. (The charge deficit vs. time revealed in the current waveform causes a max *Vout* deviation of only 13mV.)

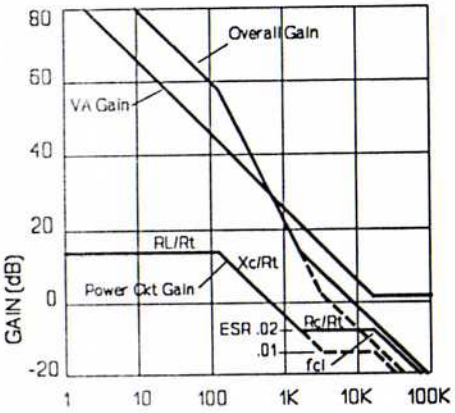

Fig. 8 - Voltage Loop Bode Plot

This demonstration is identical to the earlier current loop demonstration, except that the voltage at the CA input which programs the current is the output of the voltage error amplifier, v_{VA}. During the time the control circuit is "in the stops" while the inductor current slews to its new value, the feedback capacitor *Cfv* around the VA also charges to a voltage offset. This further increases the I_L overshoot, which now almost exactly cancels the earlier charge deficit.

After the current transition from 15A to 20A load has been completed, a 2:1 line voltage change is demonstrated. At 100µsec, the input voltage is changed instantaneously from 7V to 14V. Note how the duty cycle is reduced in the very first switching cycle. The longer OFF time increases inductor ripple current and the V_{CA} ripple, but the slopes at the PWM input remain nearly coincident as seen in the upper waveforms.

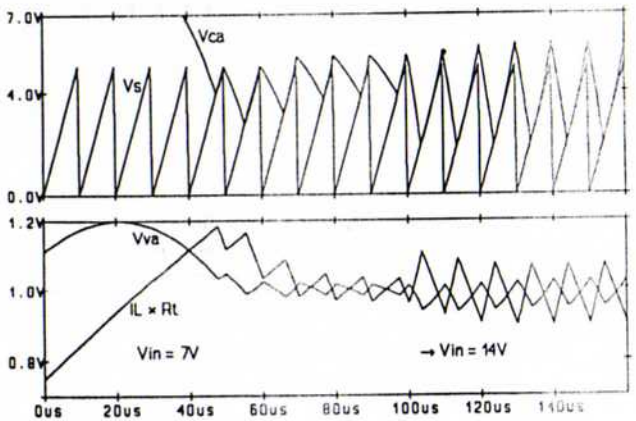

Fig. 9 - Waveforms with Load and Line Changes

Flyback with Average Current Mode Control

Fig. 10 is the circuit diagram of a flyback regulator operating in the continuous inductor current mode. Fig. 11 is the corresponding Bode gain plot.

Conditions:

$Vi = 6 \rightarrow 12V$	$Vo = 5V$	$L = 1.375\mu H$
$C = 50.000\mu F$	$Rc = .002$	$Io = 20A$
$Rt = .05\Omega$	$Vs = 5V$	$fs = 100kHz$

Description: The flyback topology is popular because of its simplicity, having one magnetic device which is also capable of providing isolation. Discontinuous flyback operation is simple, but suffers from high peak secondary current—80A for a 20A output. When the power switch turns off, 80A peak is suddenly delivered to the output, putting a tremendous burden on the output filter capacitors. Continuous mode operation can almost halve this peak current, easing the burden on the output capacitors.

The big problem with continuous mode flyback circuits is the right half-plane (RHP) zero which appears in the loop gain characteristic. The crossover frequency, fc must be well below the RHP zero frequency. This is more difficult because the RHP zero moves considerably with load and with Vin. The designer's dilemma is that if the inductor is made large to remain in continuous conduction at light loads, the RHP zero frequency is very low. If the inductor is made small, the circuit cannot be operated with light loads, because the loop gain drops too much when the mode boundary is crossed.

Average current mode control helps solve this problem in several ways: (1) It controls average output (diode) current, thus the RHP zero is dealt with and "buried" in the current loop. (Conventional current mode control controls the wrong current—inductor current—and does not deal with the RHP zero. (2) Because of the gain provided by the current error amplifier, the current loop can operate across the mode boundary and maintain acceptable regulation. This allows the inductor to be smaller (limited only by higher peak current considerations), which raises the RHP zero frequency permitting a

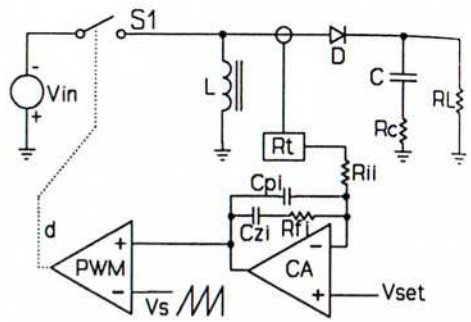

Fig. 10 - Flyback Avg. Output Current Control

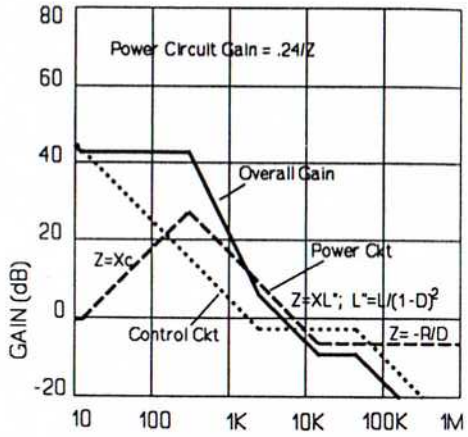

Fig. 11 - Flyback Bode Plot

higher crossover frequency.

There are two unique considerations in the design of the average current mode control loop for the flyback circuit. First, the *diode* current is being sensed, averaged and controlled, not the inductor current. The diode current is a large amplitude essentially rectangular waveshape. It is necessary to integrate this waveform to obtain its average current. The integrating capacitor, *Cpi*, added to the CA feedback network must be small or it would hurt the loop bandwidth. The CA output has a sawtooth ripple component from the integration, analogous to the sawtooth inductor ripple current.

Second, the sawtooth waveform at the CA output is 180° out of phase with the sawtooth waveform seen in the buck regulator. Rather than concern about too much slope during the OFF time, the concern now is with the ON-time slope. The worst-case ON-time slope should be 1/2 the slope of sawtooth voltage *Vs*.

Implementation:

Sawtooth slope:

$$dv_S/dt = Vs/Ts = 5V/10\mu sec = 0.5V/\mu sec$$

During the ON time, the voltage across transresistance *Rt* is zero, so V_{SET} is across the 50K integrator input resistor *Rii*. The integrator is set up for $dv_{CA}/dt = \frac{1}{2}dVs/dt$ under worst case condition of $V_{SET}max = 1.2V$ (corresponding to current limit).

$$\max I_{Rii} = \frac{V_{SETmax}}{Rii} = \frac{1.2V}{50K} = .024mA$$

$$Cpi = \frac{\max I_{Rii}\, 2T_s}{V_s} = 100pF$$

The minimum RHP zero frequency occurs with min *Vin* and min load resistance. (D = *Vo/(Vi+Vo)*)

$$f_{RHPZ} = \frac{(1-D)^2 R_L}{D \quad L} = 14.5\,kHz$$

Since there is so much excess phase shift associated with the RHP zero, we will steer clear of it and cross over at 5 kHz. The PWM/power circuit gain at 5kHz is:

$$\frac{v_i}{v_{CA}} = \frac{Vin}{V_S}\,\frac{Rt}{D(1-D)\,Z}; \quad \text{where } Z = X_L'' = \frac{2\pi fL}{(1-D)^2}$$

$$\frac{v_i}{v_{CA}} = 1.39$$

The CA gain must be flat from *fc*/2 to well above crossover to maintain an overall -1 slope. To cross over at 5kHz, the CA gain must be the reciprocal of the PWM/power circuit gain:

$$\frac{V_{CA}}{V_i} = 1/1.39 = 0.719$$

$$Rfi = 0.719\,Rii = 0.719 \times 50K = 36K$$

A pole at *fc*/2 (2500Hz) provides a -2 slope for low frequency gain boost:

$$Cfi = \frac{1}{2\pi f Rfi} = 1768\,pf$$

Some Practical Control Loop Problems

Compensation Capacitor Problems: It is usually essential to use capacitors in compensation networks around the error amplifiers in the control loop. Compensation capacitors which break the DC path between op-amp input and output operate with a DC bias voltage. This is not a problem under strictly small-signal operating conditions. But when line or load changes occur, or during startup, the amplifier output voltage must change. This requires a change in the DC bias across the series compensation capacitors. The charging current required can cause significant errors or delays in the transient response of the power supply.

Small capacitors with short time constants which provide high frequency compensation (such as adequate phase margin at crossover) don't usually cause problems. The problem is with larger capacitors (with long time constants) which are put in series with the feedback path around the amplifier for two reasons: (1) To break open a DC path around the amplifier which is causing a DC offset error, or (2) To boost the low frequency gain to obtain near-perfect regulation.

Transient behavior: What is the good of improving the DC regulation if the transient response is hurt? (The answer might be that your customer only looks at DC regulation.) Consider what happens with a significant and rapid load change. Without the series capacitor, there will be a DC path around the amplifier and finite DC gain. Assume that the output voltage changes from 5.1V with light load to 5.0 volts at full load. A series capacitor provides a low frequency zero which greatly improves regulation. Assume perfect regulation: 5.0V at light and at full load. But when the load suddenly decreases, Vout *will* swing momentarily to 5.1V, then return precisely to 5.0V. Later, when the load suddenly increases, Vout *will* swing

momentarily to 4.9V, then return precisely to 5.0V. The output voltage envelope is twice as great with the capacitor as without it.

So think twice about adding a low frequency zero just for the sake of DC regulation. If the gain is too low without the boost capacitor, look for ways to optimize the loop gain by some other method, such as optimizing the compensation scheme.

If a series capacitor is essential, make sure the output voltage swing of the op-amp is restricted in some way. Otherwise, the series capacitor can charge to a large offset voltage during startup or other transient conditions, thus taking a longer time to recover. If the op-amp output is not internally clamped, apply an external clamp. A transconductance amplifier is easy to clamp directly across the output. Any amplifier can be clamped with a Zener diode from output to inverting input. Leave 1 or 2 Volts headroom for AC components riding on the control signal.

DC current offsets: When there is DC resistance between op-amp input and output, there will inevitably be DC error caused by current flow through this resistance. In exercising control throughout the full range of operating conditions, the op-amp output must swing over a range of voltages. The current offset error is minimized by biasing the op-amp inputs at a DC voltage exactly in the middle of this output voltage range. There will be no current offset error when the output is in the middle of this range, but there will be ± regulation error at the operating extremes.

For example, if the control IC permits, divide down the reference voltage applied to the non-inverting op-amp input so that its voltage is at the mid-range of the output swing. This is a good practice even when a series boost capacitor is used, because the capacitor bias voltage will be close to zero, requiring no time to charge at start-up.

If the op-amp voltage is fixed internally, consider canceling the mid-range DC offset current by providing a compensating current to the op-amp input.

Amplifier bandwidth limits: Needless to say, if the compensation scheme requires more gain at high frequency than the op-amp can provide, there's a problem. One such problem area is the current amplifier in an average current mode control loop. In order to minimize power dissipation in the current sense resistor, it is desirable to use a very small resistance value. Although the op-amp input offset spec may be low enough to permit a very small sense voltage with reasonable accuracy, the small sense voltage will require more op-amp gain-bandwidth than nay be available..

Noise filtering: High frequency poles are often added in a control loop to attenuate noise spikes that might otherwise propagate through the loop, causing spurious turn-on and unpredictable operation. In general the pole frequencies should be at least 2-3 times *fs*, to avoid signal distortion and impaired response to sudden overloads, for example. This is especially important with conventional peak current mode control, which is very noise sensitive, but also sensitive to the effects of waveform distortion caused by over-filtering.

References:

[1] R. D. Middlebrook, "Topics in Multiple-Loop Regulators and Current-Mode Programming," *IEEE PESC*, June, 1985

Design Reference Addenda