IEICE TRANS. ELECTRON., VOL. E80-C, NO. 12 DECEMBER 1997

PAPER Special Issue on Low-Power and High-Speed LSI Technologies

A 100 MIPS High Speed and Low Power Digital Signal Processor

Hiroshi TAKAHASHI†a), *Member*, Shigeshi ABIKO†, Shintaro MIZUSHIMA†, Yuji OZAWA†, Kenichi TASHIRO†, Shigetoshi MURAMATSU†, Masahiro FUSUMADA†, Akemi TODOROKI†, Youichi TANAKA†, Masayasu ITOIGAWA†, Isao MORIOKA†, Hiroyuki MIZUNO†, Miki KOJIMA†, Giovanni NASO††, Emmanuel EGO†††, *and* Frank CHIRAT†††, *Nonmembers*

SUMMARY A 100 MIPS high speed and low power fixed point Digital Signal Processor (DSP) has been developed applying 0.45 μm CMOS TLM technology. The DSP contains a 16-bit $\times$32K full CMOS static RAM with a hierarchical low power architecture. The device is a RAM based DSP with a total of 4.2 million transistors and a new low power design and process which enabled an approximate 50% reduction in power as compared to conventional DSPs at 40 MHz. In order to cover very wide application requirements, this DSP is capable of operating at 1.0 V [1] for DSP core and 3.3 V for I/O. This was achieved by new level shifter circuitry to interface with cost effective 3 V external commodity products and confirmed 80% of power reduction at Core_V_{DD}=2.0 V, I/O_V_{DD}=3.3 V at 40 MHz. This paper describes the new features of the high speed and low power DSP.

key words: *100 MIPS, digital signal processing, high speed, low power, CPU*

1. Introduction

Very high speed (>100 MIPS), low power DSPs are required for several markets such as wireless communication terminals, base stations including FPLMTS, PDA, MODEM and HDD applications. As wireless telecommunication market grows rapidly, the number of competitors with attractive devices are increasing. Thus the market requirements become severe in terms of cost, power and speed. To meet higher performance requirement and support large production quantity, it is needed to apply advanced process. The target voltage range has been also changed to 3 V from conventional 3 V/5 V mixed support range. The characterization results show that more than 50% power reduction can be achieved by design and process optimization. In order to increase operating frequency without changing the power consumption of currently available 50 MIPS DSPs [1], further power reduction techniques must be applied. The CPU core uses a modified Harvard architecture and the CPU employs a six-stage instruction pipeline to maximize throughput. The CPU contains a 40-bit ALU, which can selectively feed one of two 40-bit accumulators shown in Fig. 1. The DSP features a multiply-accumulate (MAC) block capable of a 17$\times$17-bit two's complement multiplication and a 40-bit addition in a single cycle. The new DSP core consumes half of the power of conventional devices. This was archived by both process and design optimizations. Also in order to obtain quick TAT of the system, software debugging and flexible software updating, a very large on-chip RAM has been implemented in this DSP. The DSP contains 32 KW on-chip program/data RAM with 8 MW extended address capability for external program memory space. Four blocks of 2 KW dual access RAM and three blocks of 8KW single access RAM modules are placed in the DSP to obtain 100 MIPS operation. New hierarchical low power architecture is added since RAM is one of the modules consuming most power in the DSP [3], [4]. New level shifter circuitry is implemented to support dual voltage supply operation maintaining high speed and low power during level shift operation. These new enhancements contributed remarkablely to power reduction.

2. Power Reduction and Speed Improvement by Process

Most of power consumes in the clock circuit of the

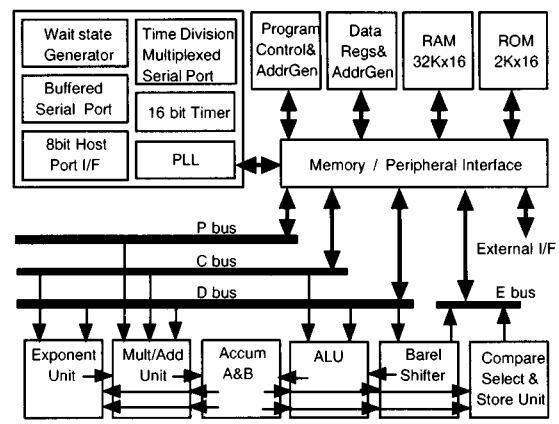


Fig. 1 System diagram of DSP.

Manuscript received April 18, 1997.
Manuscript revised August 7, 1997.

† The authors are with ASP Department, DSP Development, Texas Instruments Japan limited Tokyo, Japan.
†† The author is with Texas Instruments Italy, Avezzano, Italy.
††† The authors are with Texas Instruments France, Nice, France.
a) E-mail:hiroshi@tdc. tijp. ti.com

DSP even though the CPU core was designed with low power circuitry [1], [2]. However, by optimizing both the process and design and by focusing only on a maximum supply voltage of 3.3 V, larger power reductions were confirmed as compared to conventional DSPs, based on 5 V and 3 V supply voltages. The lower voltage device specification allowed a further shrink in the technology while keeping adequate break down voltage and I-off current performance. The technology used was an 84% shrink from 0.6 μm to 0.45 μm, with gate oxide thickness decreased from 8.5 nm to 7.5 nm. Additionally, the metal system was changed from CVD-W to AlCu/TiN. This led to the reduction of sheet resistance from 150 mOhm/square to 50 mOhm/square. As a results, buffer transistor size was drastically reduced and clock and bus driver tree networks were optimized. These optimizations contributed to a 24-48% power reduction in the CPU core as shown in Fig. 2, where pattern-A is an application test pattern to get maximum power and pattdrn-B is EXECUTE-NOP. Moreover, a process which offered a 50% larger I-drive current was selected for this DSP to maximize speed even though I-off leakage current of each transistor increases from 10 pA/um to 1 nA/um, I-drive of Pch transistor increases from 175 μA/um to 250 μA/um and I-drive of Nch transistor increases from 400 μA to 520 μA/um. This choice was based on the fact that most of the target applications require higher MIPS rather than lower stand-by current, such as wireless communication. In the case of a wireless communications terminal, system level power down is already applied without usage of DSP stand-by mode (IDLE-3). Additionally, base station application does not use this mode since the system is never turned off during normal operation. These changes in process resulted in remarkable speed improvement while providing a 20% power reduction at 40 MIPS as compared to conventional devices operated under identical conditions.

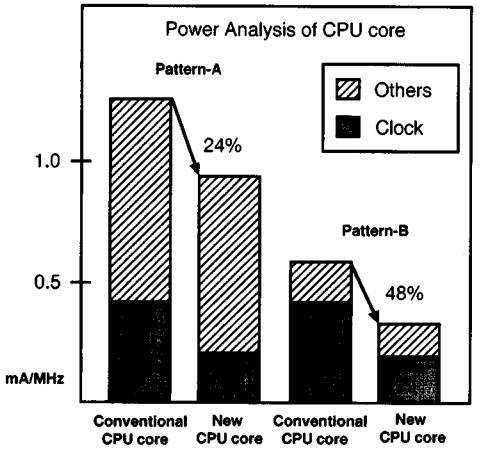


Fig. 2 Power reduction of CPU core.

3. Clock and Bus Power Reduction and Speed Improvement

In conventional designs, the master clock of the Scannable Register Latch (SRL) is controlled by the Gated Clock Driver (GCD). But the slave clock of SRL is not controlled and is free running. To address this issue, a novel circuit, the Gated Slave Logic (GSL) was developed as shown in Fig. 3 and Fig. 4 [2]. This GSL reduces the slave clock (vst) transitions. Figure 3 shows the diagram with shift registers and GSL and timing chart. Figure 4 also shows the gate slave logic circuitry. Functional blocks are only clocked when they have valid data to process. Transition of the data inputs to a functional block activates a data ready signal, which is used to locally gate the master clock.

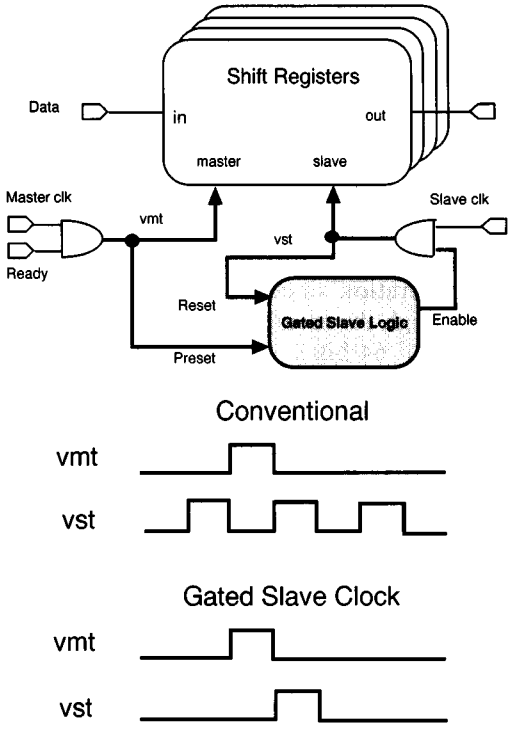


Fig. 3 Gated Slave Logic diagram and data shift register.

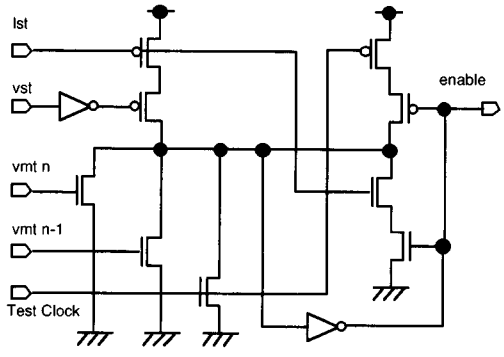


Fig. 4 Gated Slave Logic circuit.

The GSL can control many SRL inputs and the SRL can have many data keep conditions. This additional circuit did not impact layout density. As a result, the GSL was applied to 28 slave clock lines with 504 SRLs in the CPU core and about 50% of slave clock was disenabled. Adding this new GSL and clock buffer size reduction with other minor modifications, a power reduction of about 17% was achieved as compared with conventional CPUs.

4. Low Power and High Speed Memory Design

The DSP contains 24 kW single access and 8 kW dual access memory. In order to reduce power and achieve 100 MIPS operation, the memory has been segmented into three blocks of 8 kW modules for single access and four blocks of 2 kW modules for dual access. During memory access, only one of the memory modules will be activated, which resulted in power reduction. Moreover, 6 transistor 38 μm**2 full CMOS static RAM is used and metal-1 is used for polycide word line strap to reduce the RC delay of word line. The smaller memory cell reduced parasitic capacitance of the bit lines and word lines which also contributed to power reduction. The new hierarchical low power architecture was also applied as shown in Fig. 5. Conventional arrays dissipate more power during precharge operation since all of the bit lines are discharged through the memory cell during the word line activation (All 64 bits). A new hierarchical memory only accesses the necessary 16 bits (1 word) by decoding the global word line and block select signal, thus eliminating the discharge of the 48 unnecessary bit lines (64-16 bit). Since the local word lines which are not used stay at a low state, and bit and xbit line are kept in a high state, the memory does not consume power for precharging these bit lines. In this new architecture, 16 global bit lines are used commonly by the read and write circuitry. Grounded shield lines were added to each global bit line to eliminate cross talk of signals caused by the large coupling capacitance of the long parallel wiring. Sense amplifier input differential voltage requires 5-10% of V_{DD} voltage to ensure adequate noise margin and sensitivity. About 50% of the capacitance in the global bit line was due to line to line coupling. The bit line signal swing at read operation is about 400 mV at V_{DD}=3.0 V and worst case cross talk reduces differential voltage at the sense amplifier input as shown in Fig. 6. The worst case cross talk occurs when the sensing signal stays high and both lines go low, in which case the differential voltage at the amplifier is reduced by AC coupling. By adding a grounded shield line cross talk can be greatly minimized and faster operation speed is possible due to fast sense amplifier enable signal timing at 150 mV differential voltage. Speed improvement in RAM, especially the 2 kW dual access RAM, is very important to allow 100 MIPS operation, since RAM is the critical path in conventional DSP rather than data path in CPU core. To eliminate signal transition delay by cross talk is important for chip level buses, clocks and other key signal lines adding shield line effect, considering signal transition phase and line to line coupling ratio. These routing management could minimize unexpected delay by cross talk effect in signal transition, especially between memory and CPU core. The addition of logic for low power and grounded shield line for high speed resulted in 9% increase of the module area but reduced power by 33% during the read operation and 35% during the write operation.

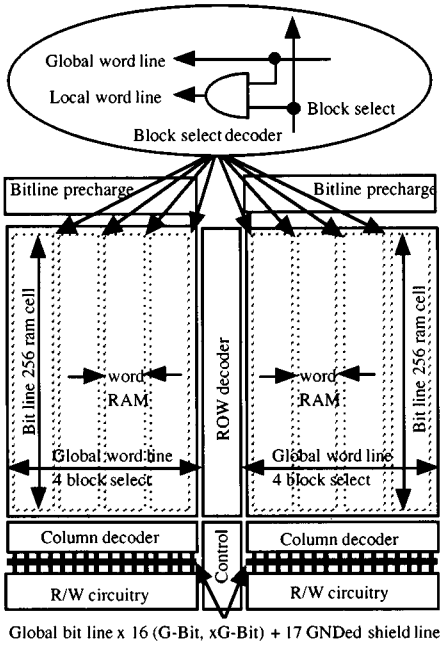


Fig. 5 New hierarchical architecture memory.

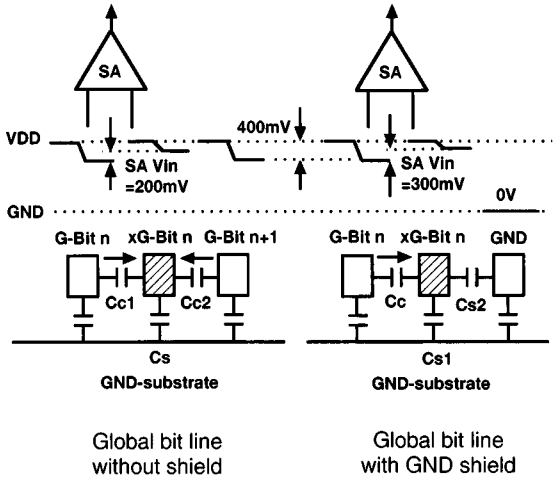


Fig. 6 RAM global bit line shield effect.

5. High Speed Low Power Level Shifter Circuitry

New I/O circuitry to support dual voltage supply operation was developed to interface with 3.3 V external devices. The DSP can operate at less than 1.0 V with minimum speed degradation due to the newly developed high speed and low power level shifter circuitry. New level shifter circuits include NAND/AND, OR/NOR function to control the tri-state output buffer. The conventional AND/NAND type and new level shifter circuitry are shown in Fig. 7. The conventional level shifter requires 10 transistors and the new one requires 14 transistors. However, in the conventional level shifter, the *N*ch devices used were 4 times bigger than the *P*ch devices since low voltage input to *N*ch device *I*-drive was reduced. The conventional level shifter has a large short circuit current during level shifting operation since the level shift from low to high voltage needs to discharge the output node which is fed back to the Pch driver devices to turn them on and off. A larger *N*ch device was required for faster level shift operation to minimize signal conflict between High Voltage (HV) and GND through *P*ch driver and *N*ch discharge transistors. The new level shifter circuitry reduced these short circuit currents and improved the speed of level shifting. *P*ch devices are added between *P*ch driver devices and *N*ch discharge transistors. These additional *P*ch devices act as current limiters since input voltage swing is small due to Low Voltage (LV). For example, when HV is 3.3 V for external interface and 1.0 V for DSP core voltage, *P*ch V_{gs} is 0 V–1.0 V and remarkably reduces *P*ch device *I*-drive at 1.0 V input. As a result, the *N*ch device ratio was reduced from 5 to 2 getting two and half times faster level shift operation speed. A comparison table of the conventional and new buffer type level shifter is shown in Fig. 8. This new circuitry is usable for buffer type, OR/NOR type, and complex gate type of circuit combinations. This new capability led to remarkable power reduction as compared with conventional DSPs. When HV is set to 3.3 V and LV set to 2.0 V, the new DSP can operate at 40 MIPS and power consumption is just 20% of conventional DSP at the same testing condition. In other words, 80% of the power consumption is reduced by this new dual voltage supply capability.

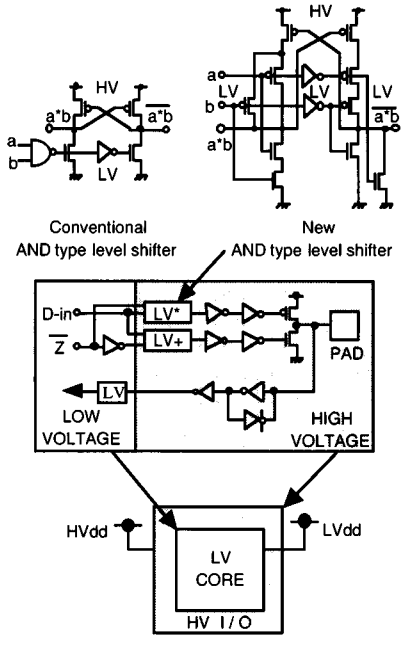


Fig. 7 I/O buffer with level shifter circuitry.

	Conventional level shifter	New level shifter
Speed	1.0	1.0
Area	1.0	0.82
Power	1.0	0.77

Fig. 8 Comparison of level shifter circuit.

6. Conclusion

A 100 MIPS RAM based DSP has been developed with remarkable power reduction and speed improvement achieved by both process and design optimization. Compared to conventional DSPs, a power reduction of about 50% was observed under the same testing conditions. The key feature of this device are summarized in Table 1. The typical power-performance metric of the new DSP was 0.7 mA/MHz as compared with 1.3 mA/MHz for a conventional DSP. Additionally the new DSP could be operated at twice the frequency without major changes in power consumption. This typical power-performance metric assumed a REP-MAC

Table 1 Comparison of conventional DSP vs New DSP.

	Conventional DSP	New DSP
Technology	0.6um CMOS	0.45um CMOS
Gate Oxide	8.5nm	7.5nm
I-drive (Pch)	175uA/um	250uA/um
I-drive (Nch)	400uA/um	520uA/um
I-off current	10pA/um	1nA/um
Metal Resistance	150mOhm/Square	50mOhm/Square
Transistors	1.6 M	4.2 M
Package	100/128 TQFP	144 TQFP
Maximum Speed	50MHz	100MHz
Power-Performance	1.3mA/MHz	0.7mA/MHz
IDLE-1	0.25mA/MHz	0.12mA/MHz
IDLE-2	0.05mA/MHz	0.03mA/MHz
IDLE-3	100nA	100uA

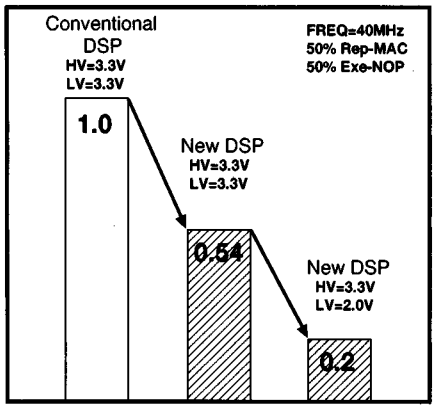
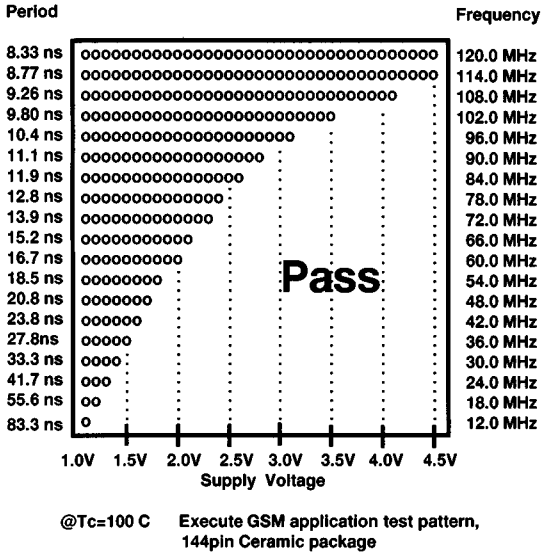


Fig. 9 Power comparison of conventional DSP and new DSP.

Table 2 Schmoo plot of new DSP.



@Tc=100 C Execute GSM application test pattern, 144pin Ceramic package

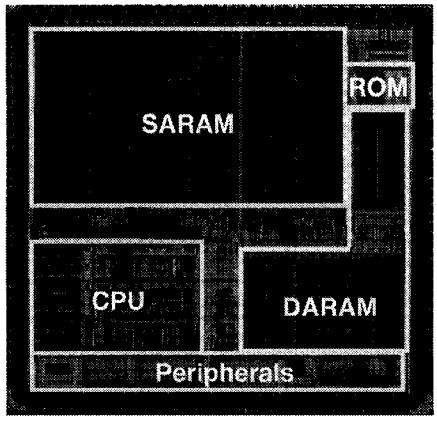


Fig. 10 Chip micro graph of new DSP.

instruction (50%) and EXECUTE-NOP instruction (50%). The new DSP is capable of operating at HV=3.3 V, LV=2.0 V and consumes only 20% the power (at 40 MHz) of conventional DSPs as shown in Fig. 9. In case of HV=LV=3.4 V, 100 MHz and HV=LV=1.0 V, 10 MHz operation is possible shown in Table 2. The DSP has power down instructions which are IDLE1 to shut down the CPU, IDLE2 to shut down the CPU and the on-chip peripherals (except PLL) and IDLE3 to shut down the entire processor. Chip photograph is shown in Fig. 10. The flexibility and wide operating margin greatly increase the applications opportunity of this new DSP.

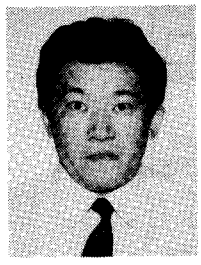
References

[1] H. Takahashi, S. Abiko, S. Mizushima, and Y. Ozawa, "A circuit library for digital signal processor," Special issue on low power and analog, digital LSIs and ASICs for multimedia, IEICE Trans. Electron., vol. 78-C, no. 12, Dec. 1995.

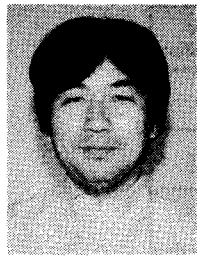
[2] W. Lee, P. Landman, B. Barton, S. Abiko, H. Takahashi, H. Mizuno, S. Muramatsu, K. Tashiro, M. Fusumada, L. Pham, F. Boutaud, E. Ego, G. Gallo, H. Tran, C. Lemonds, A. Shih, M. Nandakumar, B. Eklund, and I.C. Chen, "A 1V DSP for wireless communications," ISSCC Digest of Technical Papers, pp. 92-93, Feb. 1997.

[3] H. Kabuo, M. Oakamoto, I. Tanaka, H. Yasoshima, S. Marui, M. Yamasaki, T. Sugamura, and K. Ueda, "An 80-MOPS-peak high speed, and low power-consumption 16-b digital signal processor," IEEE J. Solid-State Circuits, vol., 31, no. 4, April 1996.

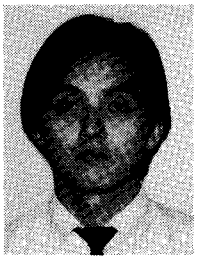
[4] M. Yoshimoto, H. Shinohara, T. Yoshihara, H. Takagi, S. Nagano, S. Kayano, and T. Nakano, "A divided word-line structure in the static RAM and its application to 64 K full CMOS RAM," IEEE J. Solid-State Circuits, vol. 18, no. 5, pp. 479-485, Oct. 1983.



Hiroshi Takahashi was born in Saitama, Japan on November 11, 1959. He graduated from Shohoku College, (Sony Gakuen) Kanagawa, in 1980, his major was electronics. In 1980, he joined Dai-Nippon Printing Inc and worked at CAD section. In 1984, He joined Texas Instruments Japan Ltd., He was been engaged in DSP design since 1985 and developed several DSP devices include EPROM version at TI France and TI U. S. A. He is a Senior Member Group of Technical Staff (SMTS) in TI and member of IEEE.

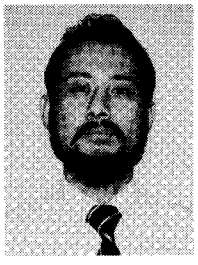


Shigeshi Abiko was born in Chiba, Japan on July 30, 1959. He received the B. S. degree in computer science from the Scientific University of Tokyo, Japan, in 1982. He joined the Tokyo Design center, Texas Instruments Japan Ltd., Tokyo, Japan, in 1982, and then worked on the development of programmable DSP devices. He is a Senior Member Group of Technical Staff (SMTS) in TI and member of IEEE.

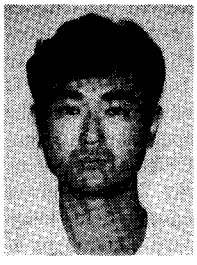


Shintaro Mizushima was born in Okayama, Japan on January 27, 1961. He received the B. S. degree in electronics from Aoyama Gakuen University, Japan, in 1984. He joined the Tokyo Design Center, Texas Instruments Japan Ltd., Tokyo, Japan, in 1984, and then worked on the development of custom and programmable DSP devices.

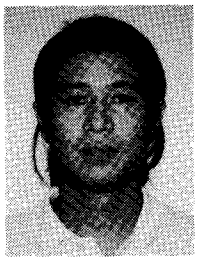
Akemi Todoroki was born in Nagano, Japan on October 2, 1966. She graduated from Tokyo Kougakuin College Tokyo, Japan, in 1989. She joined the Tokyo Design Center, Texas Instruments Japan Ltd., Tokyo, Japan, in 1989, and then worked on the development of custom DSP and programmable DSP devices.



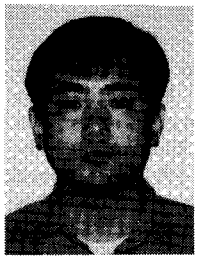
Yuji Ozawa was born in Gifu, Japan on September 8, 1961. He received the B. S. degree in physics from Shinshu University, Japan, in 1985. He joined the Tokyo Design Center, Texas Instruments Japan Ltd., Tokyo, Japan, in 1985, and then worked on the development of custom and programmable DSP devices.



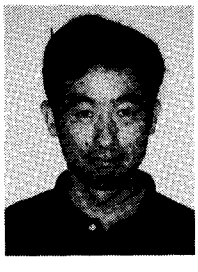
Youichi Tanaka was born in Tokyo, Japan on December 24, 1966. He received the B. S. degree in electronics from Tokyo Denki University, Japan, in 1990. He joined the Tokyo Design Center, Texas Instruments Japan Ltd., Tokyo, Japan, in 1990, and then worked on the development of custom and programmable DSP devices.



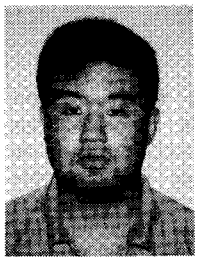
Kenichi Tashiro was born in Osaka, Japan on January 30, 1965. He received the B. S. degree in electronics from Osaka Institute of Technology, Japan, in 1987. He joined the Tokyo Design Center, Texas Instruments Japan Ltd., Tokyo, Japan, in 1987, and then worked on the development of custom and programmable DSP devices.



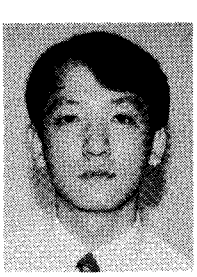
Masayasu Itoigawa was born in Gifu, Japan on January 13, 1970. He received the B.S. degree in electrical engineering from Aichi Institute of Technology University, Japan, in 1992. He has been joined Texas Instruments Japan, working on the development of 1-bit DA converter and programmable DSP devices.



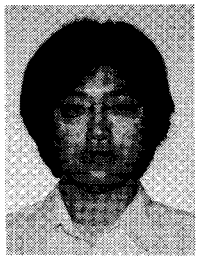
Shigetoshi Muramatsu was born in Nagano, Japan on March 11, 1964. He received the B. S. degree in applied physics from Nagoya University, Japan, in 1987. He joined the Tokyo Design Center, Texas Instruments Japan Ltd., Tokyo, Japan, in 1987, and then worked on the development of DA converter at R & D in TI Dallas, U. S. A. and custom DSP and programmable DSP devices. He is member of IEEE.



Isao Morioka was born in Toyama, Japan on March 29, 1971. In 1992, he joined Texas Instruments Japan Ltd., where he graduated from Nippon Electronics College, Tokyo, his major was Artificial Intelligence. He has been joined Texas Instruments Japan, working on the development of 24-bit audio DSP and programmable DSP devices.

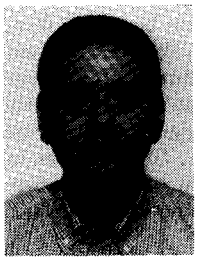


Masahiro Fusumada was born in Buenos aires, Argentine Republic on July 19, 1964. He received the B. S. degree in physics from Tokai University, Japan, in 1987. He joined the Tokyo Design Center, Texas Instruments Japan Ltd., Tokyo, Japan, in 1987, and then worked on the development of 24-bit audio DSP, custom and programm-able DSP devices.

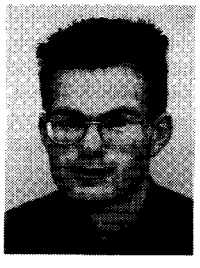


Hiroyuki Mizuno was born in Aichi, Japan on February 23, 1969. He received the M. S. degree at the Department of Materials Science and Metallurgy, University of Tokyo, Japan, in 1994. He joined the Tokyo Design Center, Texas Instruments Japan Ltd., Tokyo, Japan, in 1994, and then worked on the development of programmable DSP devices.

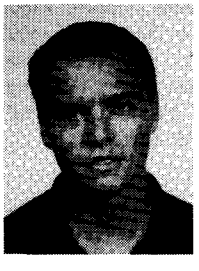
Miki Kojima was born in Aichi, Japan on December 17, 1968. She attended Barnard College, Columbia University. She joined Tsukuba R & D center Texas Instruments Inc, in 1991. She joined Design Center Design Automation Division, Texas Instruments Japan Ltd, in 1992. She has been working on the development of timing and power analysis environments for DSP design.



Giovanni Naso received his master degree in electronics engineering from Rome University (Italy) in 1983. In 1987, he joined Texas Instruments R & D department. He worked two years in the nonvolatile memory department in Houston developing flash EEPROM memories. He has been a designer in automotive EPROM Memories and in Field Memories projects. His last assignment is leader of Italian team for DSP embedded SRAM. Giovanni is Member Group of Technical Staff (MGTS) at TI and member of IEEE.



Emmanuel Ego was born in Cambrai, France in 1969. He received his engineer degree in microelectronics from Institute Superieurd' Electronique du Nord, Lille, France in 1992. He joined Texas Instruments France in december 1994. He has been designing PLLs for DSPs circuits since then. He is now involving in design of digital blocks to be integrated in next generation of low-power programmable DSP cores.



Frank Chirat was born in Saint Etienne, France in 1969. He received his M. S. degree in electronics from Institute National polytechnique de Grenoble (INPG). Since January 1996, he has joined Texas Instruments France working on DSP devices as a Test and Product Engineer.