THPM 20.7

A 2.9 Megabit Field Memory for IDTV and PAL+ applications

Elio d'Ambrosio, Maurizio Fragano, Giuliano Imondi,
Mario Lanciano, Stefano Menichelli, Giovanni Naso

Research & Development Department, Texas Instruments Italy

ABSTRACT - Today's television has reached a high state of picture quality, and further major improvements are limited by the restrictions of the transmission standards. However, as IC technology advances, means have become available to eliminate or reduce many of the effects which still impair a perfect picture rendition. Among these effects are large-area flicker, line-flicker, cross talk between luminance and chrominance, and noise.

Most of the TV makers working in that application area, normally referred to as IDTV (Improved Definition TV), use dedicated ASM, called Field Memories (FMEM's), to store in an appropriate digital format the picture received by the TV set, and to apply to it DSP concepts, in order to improve the above mentioned effects.

A novel architecture of a 2.9Meg Field Memory that is emerging as a European Industry Standard in IDTV applications, is described. Further evolution of the device especially suitable for PALplus applications is also described.

I - *Introduction*

A Field Memory (FMEM) is a synchronous serial access memory, that operates according to the First-In First-Out (FIFO) data management concept, providing N-bit in parallel both in writing and in reading mode. While write and read operations are synchronous with the related clocks, the two clocks may be uncorrelated if so desired by the user. When read access is delayed relative to write access, the device functions like a FIFO register. The amount of delay determines the "length" of the FIFO register.

A FMEM is basically made by a DRAM memory core that, by means of an input and an output serial register and an internal refresh circuitry, acts as a fully static FIFO. However, unlike a conventional FIFO data may be read as many times as desired, once it is written into the DRAM storage array.

FMEM's are designed especially for Video and TV applications, since their first characteristic is the capability of being operated at a high speed, with clock frequency from 30 to 40 MHz.

II - *2.9 Megabit Field Memory* [*] *Architecture*

This device is a 2.9 Mbit memory that writes and reads exclusively through two serial access ports, both 12 bits wide. Each port has separate control pins and separate clocks (asyncronous operations). An internal dedicated logic provides to arbitrate all the asyncronuos requests to access the main data memory.

In order to achieve high density, dynamic storage cells (based on 4Mb DRAM technology) are employed into the core. However, the device is provided with an internal refresh circuitry that restores its storage cells automatically, so that it appears fully static to the user. Maximum storage capacity is 245,760 words x 12 bits.

As described in figure, internal write and read static data registers are used as an interface between the dynamic core memory and the serial ports. The data registers are organized in a pipeline fashion to achieve high speed performances required for IDTV applications (read and write tCYCLE min = 26ns / tACC max = 21ns).

A special function (Write Mask) acts at word level allowing the user to enable or disable writing data into the memory, thereby preserving the previous contents of the memory while the write clock and the address counter continues to run. In this way, a part of the screen picture can be updated while the other part may remain the same. The function is implemented using a novel "read-before-write" concept. Any time new data have to be stored into the memory core, the old data is previously read out from the core and, according to an auxiliary write mask information related to each word, the old data overwrites or not the new one just before the data storage into the memory.

In order to achieve a fast read/write cycle time, data registers have been used between I/O buffers and the memory core, allowing to access the storage cells with 80 words (x 12 bits) all at once. Those data registers represent a cache memory useful both in write and in read operations.

The memory core is fragmented in 8 blocks. Each of them contains 3 mini-arrays supplied with relative sense-amplifiers. On the lateral sides of each block are lined up 2 banks of registers, so that there are 16 banks in the whole core. Each bank contains a number of data registers sufficient to store 5 words, with a duplicated architecture in each register for write and read operations. The twelve bits composing a word are stored into adjacent registers to which is linked an input data bus and an output data bus, both 12 bits wide, to connect pipeline and registers.

The 16 banks of data registers are addressed by using SAP (Select Address Pointer) signals. The selection occurs independently for write (WSAP) and read (RSAP) operation. Close to each bank is aligned a group of pointers which allow the selection of one of the five words contained into each bank. Thanks to this architecture it is possible to comprehensively manage 4 words in parallel. Write pipeline makes parallel the serial input data, reducing by a factor four the frequency of the external write-clock, moving the data through the pipeline from the input buffer to the register. In a similar manner, the read pipeline makes serial the data, moving them from the registers to the output buffers, with an increase by a factor four of the frequency.

There are 5 types of operations that involve a memory core access, they are: RESET WRITE, SEQUENTIAL WRITE, RESET READ, SEQUENTIAL READ, REFRESH. All of those may happen in a time-frame defined by the time needed for writing or reading the internal data registers 80 words long. The device is provided with an arbitration logic to properly handle the core access by using a polling technique, in order to avoid conflicting problems due to contemporaneity of requests. Moreover, the arbiter assures a real time execution of all the memory accesses, by killing in critical cases (e.g. sequential read in presence of reset read) pending unusefull requests.

[*] TMS4C2970 - 2.9 FMEM by Texas Instruments Inc.

0-7803-1453-0/94 $3.00

III - *Mini cache memory implementation*

The pipeline chain located between the input/output ports and the internal data registers involves an intrinsic delay during the transitions (i.e. immediately after a reset command), both in reading and in writing mode, which is incompatible with the device's required functionality. The inconvenience has been overcome furnishing the device of a small, dedicated memory, implemented by 2 circle shift-registers for each bit of the word, one for writing (master) and one for reading (slave). Each shift register is 12 bits long. This added memory has been called "mini-cache memory" and it operates only after a reset operation for just 12 clock's shots. After a reset write, regardless of the external serial write clock, the previous write operation is completed by transferring the last old input data into the memory core using an internal clock. In the meantime, the first new 12 input words are transferred to the mini-cache memory, while the next data is again sent to the write pipeline, previously initialized and synchronized with the external serial write clock. The new data memorized in the write shift-register is transferred, as soon as possible, to the read shift-register. At the next reset read, the first 12 words are ready to feed the output buffers without delays, while at the same time the read pipeline is being initialized, with the proper data and timing, in order to get available the successive data at the 13th external serial read clock shot.

IV - *Random Block Access for PALplus applications*

To provide a wider application spectrum to the 2.9Mbit FMEM (mainly to do it suitable for PALplus decoders applications), a new version is presently in development (March 1994). The new version features an extra addressing mode, in addition to the sequential one, the "random block access". During write and/or read reset operations, by supplying a special combination of the control signals, writing and/or reading may be directed to begin or to proceed at the starting address of any one of 3072 blocks. Block size has been chosen equal to the data register size in order to facilitate internal operations (one block = 80 words).

Once a Reset Write command is detected, a 'reset write' operation is activated to store into the DRAM core the pending data. Then the device starts writing new data into the mini-cache and the control signals are acknowledged to verify whether a random block access is requested or not. If random access has not been selected, the device resets to '000' the Write Address Counter and acts exactly like in a normal Reset Write. Otherwise, the device accepts the new block address, which is clocked in serially by using D0 input pin, in order to write the new coming data at the beginning of the new block, whose address has been previously loaded into the Write Address Counter.

The read random block access is implemented with an approach similar to that one used for the write random access. Only once a random access request is acknowledged and the new block address is clocked in, the device acts in a slightly different manner: before the first data of the new addressed block is ready to be sent to the output buffers, a memory core read access using the new block address have to be accomplished (that involves a read latency of 96 serial clock cycles).