A NOVEL SUBLITHOGRAPHIC TUNNEL DIODE BASED 5V-ONLY FLASH MEMORY

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ABSTRACT

A novel tunnel diode has been developed for high density 5V-only flash memories. The memory tunnel diode is remote from the channel, self-aligned, sub-lithographic, and scalable. This remote tunnel diode provides several advantages over a conventional tunnel diode: higher junction breakdown voltage, reduced substrate current during erase, reduced tunnel oxide area, reduced cell area, and competitive cell endurance. A 256Kb 5V-only flash memory developed incorporating this tunnel diode has excellent operation and reliability characteristics.

INTRODUCTION

Flash memory has evolved as a low cost alternative to full feature EEPROM, and a more flexible alternative to UV-EPROM, with potential applications in automotives [e.g. electronic engine control], consumer electronics [e.g. copy machines], data acquisition systems, smart cards, telecommunications, solid state disks, embedded memories, etc. Over the past few years, two viable versions of flash memories have emerged: (i) those requiring dual power supplies (12V and 5V), the higher voltage for programming the memory using channel hot electron injection [1,2,3]; and (ii) those requiring a single 5V supply in which programming is performed using Fowler-Nordheim tunnelling with internally generated high voltage [4,5,6]. This paper describes the operation and reliability of a 5V-only Flash memory based on a novel tunnel diode.

TECHNOLOGY

The ACEE (Array Contactless EEPROM) for 5V-only 256Kb Flash EEPROM has been described previously (7). The ACEE is a 1.5 um, N-twin well double level poly CMOS process. The advantages of contactless array over conventional approaches in terms of cell area reduction and manufacturability have been shown in contactless one Mb EPROM [8,9]. The CMOS periphery devices have 250A gate oxide for speed improvement, LDD structure for protection against hot electron injection, and 500A gate oxide for high voltage operation.

THE MEMORY CELL

The cell is programmed and erased by Fowler-Nordheim tunnelling - a low current approach: (i) the cell consists of a floating gate structure (defined by double poly stack process) merged with a pass gate (Fig.1). The pass gate prevents the cell from drawing current when the floating gate structure is erased into depletion and eliminates the need for the complicated erase algorithms essential for 1-T cell Flash memories. (ii) The source/drain of the cell are buried under a thick oxide and constitute the continuous buried bit lines, with one contact every 16 bits in the memory array, reducing the reliability problems of cell contacts. (iii) The tunneling oxide between the floating gate and the source is about 100A. Because of low current requirements for program and erase, the operating voltages can be generated internally from a single external 5V supply. (iv) The cell is free of read disturb whether read from source or drain side, since buried N+ junctions are graded, and channel oxide is 500A on the drain side and is 350A on the source side. A 500A oxide in the pass gate region is for internally generated high voltage operation.

The array operation is shown in Fig. 2. The disturb free programming has been designed in by controlling the electric fields across the cell dielectrics. Fig. 3 shows memory programming free of write disturb [unintended programming of an erased bit].

THE TUNNEL DIODE

In conventional EEPROM cell structures , the tunnel diode lies inside the channel [7,10]. The tunnel diode discussed here has several advantages over conventional structures [11]. (i) The tunnel region is located at and self-aligned to the N+ oxide/field oxide interface, eliminating variations in tunnel area due to misalignment and lithographic dimensional deviations encountered with a conventional tunnel diode, and allows reducing the cell area. (ii) The tunnel diode is remote from the channel area, and thus both the channel and the tunnel diode have been optimized independently. (iii) The tunnel region is scalable, has sublithographic width [0.27 um @ 1.5 um rules], and occupies only 1% of total cell area, thus reducing tunnel oxide defect failures. (iv) Gated diode junction breakdown is improved because the tunnel diode junction terminates

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under the field oxide on one side and under 350A gate oxide on the other side (Fig. 4a). Erase junctions, which terminate under 100A gate oxide, breakdown well before the onset of appreciable tunneling (Fig. 4b) resulting in hot hole assisted erase.

RELIABILITY

The simulation results of current density vs. program pulse profile and the corresponding cell endurance data are shown in Fig. 5 and 6. The profiles of VPP (program pulse) and VEE (erase pulse) play a significant role in program/erase times and array endurance for building Flash memories.

Since the tunnelling current varies exponentially with electric field, the array programmabiliy/erasablility and endurance can be influenced significantly by process variations, such as tunnel oxide thickness. The impact of the process variations has been minimized by a circuit solution. The memory cell is used to generate an "adaptive" adjustment of the programming and erase waveforms. In particular, a circuit has been implemented for pulse ramp control and pulse amplitude control (Fig. 7), so that the surge electrical stress of the tunnel oxide are minimized and the trap generation is reduced. A miniarray of bits in the array is dedicated for this purpose. During wafer testing these bits are programmed, and the initial ramp and amplitude values of VPP are stored. The programming and erase pulse waveforms are adjusted via a simple D/A converter and the effect on the main array verified through Vth measurements. The process of storing new ramp and amplitude values and verifying the effect on the array is terminated when the desired range of vth is reached.

The cell endurance characteristics through 1.5 million cycles are shown in Fig. 8. The write/erase endurance of the 256Kb memory has adequate margin through 20K cycles (Fig. 9). Fig. 10 shows excellent data retention characteristics after 20K write/erase cycles.

CONCLUSION

A reliable 5V-only 256Kb Flash memory has been demonstrated with a novel, remote, self-aligned, sublithographic, and scalable tunnel diode.

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REFERENCES

1. V.N. Kynett et al, "An In-system Reprogrammable 256K CMOS Flash Memory", ISSCC Digest of Technical Papers, 1988, pp. 132-133.
2. "SEEQ'S 512-Kbit Flash EEPROMs Support In-system Programming on 12-volt Supply" Electronics, March 17, 1988, pp. 149.
3. F. Masuoka et al,"A 256-Kbit Flash EEPROM Using Triple Polysilicon Technology", IEEE J. Solid-state Circuits, Vol.SC-22, No.4, Aug. 1987, pp. 548-552,
4. S. D'Arrigo et al, "A 5V-Only 256K Bit CMOS Flash EEPROM". ISSCC Digest of Technical Papers, February 1989, pp. 132-133.
5. T. Nakayama et al, "A 5 V-Only One-Transistor 256K EEPROM with Page-Mode Erase", IEEE J. Solid-State Circuits, Vol.24, No.4. Aug. 1989, pp. 911-915.
6. Atmel 256K (32K X 8) 5 Volt Only CMOS PEROM (Product Data Sheet).
7. M. Gill et al, "A 5 Volt-Only Contactless Array 256K Bit Flash EEPROM Technology, IEDM Digest of Technical Papers, 1988, pp. 428-431.
8. J. Esquivel et al, "High Density Contactless, Self Aligned EPROM Cell Array Technology", IEDM Digest of Technical Papers, 1986, pp. 592-595.
9. T.Coffman et al, "A 1Mb CMOS EPROM With 13.5 um2 Cell", ISSCC Digest of Technical Papers, 1987, pp. 72-73.
10. W. Johnson et al, "16K EEPROM Relies on Tunnelling for Byte-erasable Program Storage," Electronics, Feb. 28,1980, p.113
11. TI Patent.

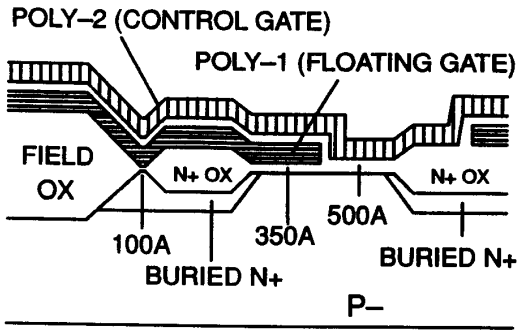


FIG 1A: ACEE memory cell cross-section with the novel tunnel diode.

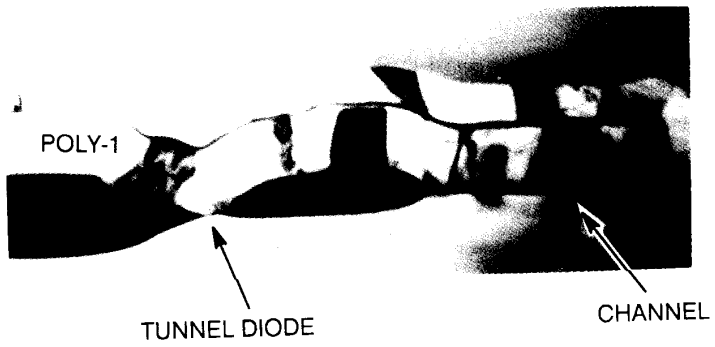
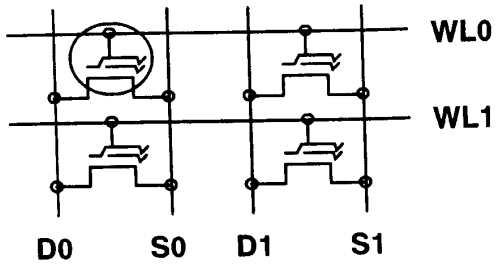


FIG 1B: TEM photomicrograph of the memory cell cross-section.



CELL (0,0) OPERATING CONDITIONS

	WL0	WL1	S0	D0	S1	D1
ERASE	-11V	-11V	5V	FLOAT	5V	FLOAT
PROGRAM	17V	7V	0V	FLOAT	7V	FLOAT
READ	3.3V	0V	0V	1.5V	0V	1.5V

FIG.2: Array operation.

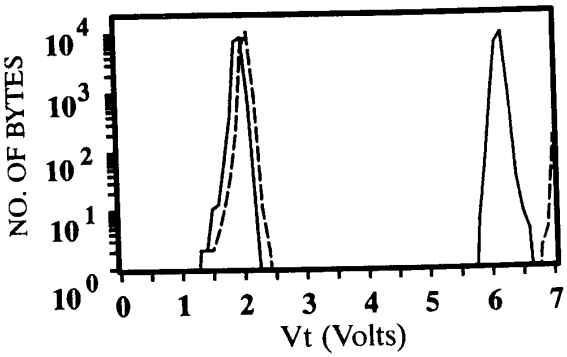


FIG.3: Repeated checkerboard programming shows excellent write disturb characteristics [256Kb memory].

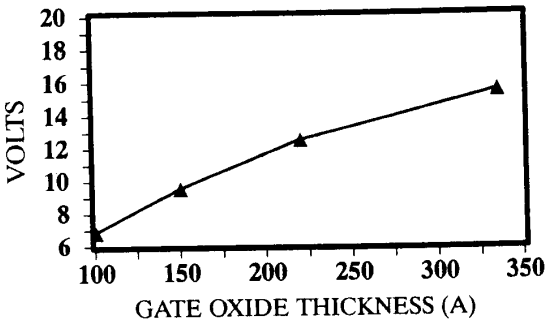


FIG.4A: Grounded gate diode breakdown voltage VS. Gate oxide thickness.

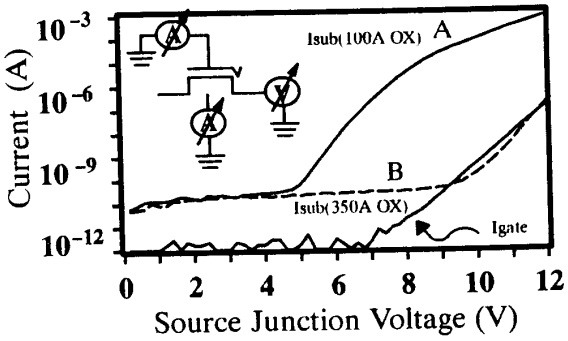


FIG.4B: Poly 1 array grounded gate I-V characteristics. (A) Conventional (local) tunnel diode with 100A gate oxide. (B) Remote tunnel diode with 350A gate oxide.

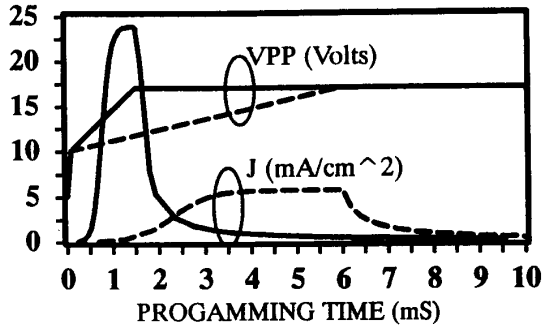


FIG.5: Simulation results of tunnel current density vs. VPP profile.

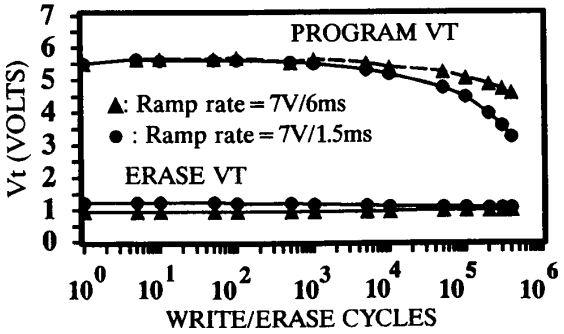


FIG.6: Discrete cell endurance with different VPP ramp rates.

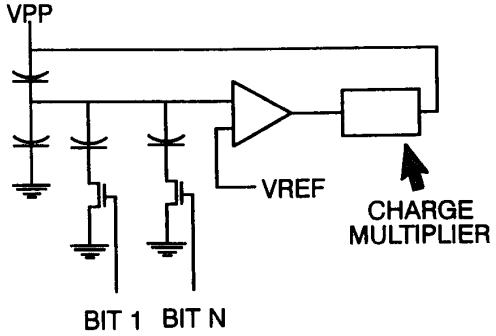


FIG.7: Circuit for adaptive adjustment of VPP/VEE amplitude and ramp rate.

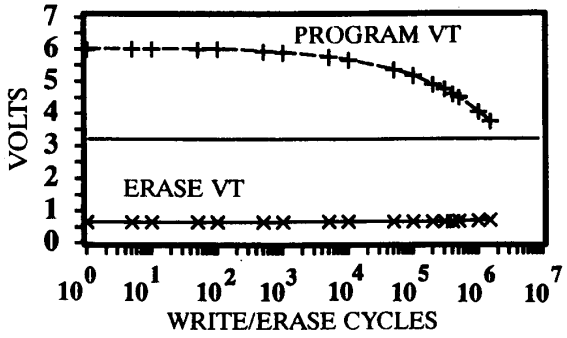


FIG.8: Discrete cell endurance characteristics through 1.5 million write/erase cycles.

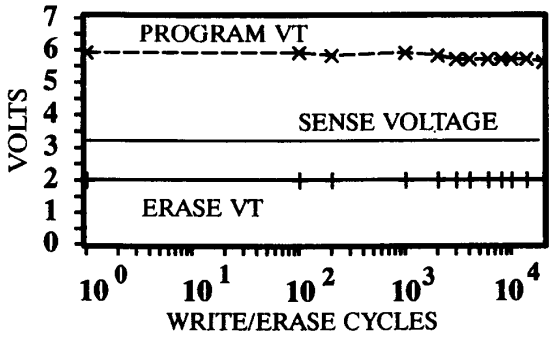


FIG.9: 256Kb memory endurance characteristics through 20K write/erase cycles.

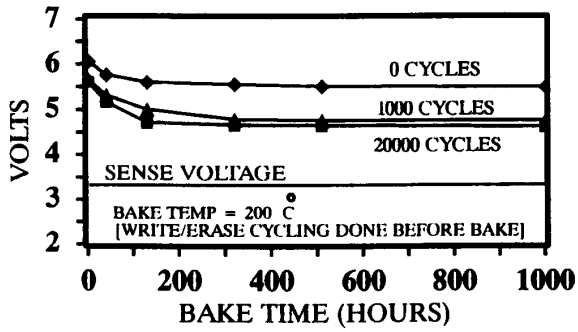


FIG.10: Data retention characteristics after 20K write/erase cycles [256Kb memory].