- A single STM instruction at subroutine entry can push register contents and the return address onto the stack, updating the stack pointer in the process.
- A single LDM instruction at subroutine exit can restore register contents from the stack, load the PC with the return address, and update the stack pointer.

LDM and STM instructions also allow very efficient code for block copies and similar data movement algorithms.

Swap register and memory contents

A swap (SWP) instruction performs the following sequence of operations:

- 1. It loads a value from a register-specified memory location.
- 2. It stores the contents of a register to the same memory location.
- 3. It writes the value loaded in step 1 to a register.

By specifying the same register for steps 2 and 3, the contents of a memory location and a register are interchanged.

The swap operation performs a special indivisible bus operation that allows atomic update of semaphores. Both 32-bit word and 8-bit byte semaphores are supported.

4.0.8 Coprocessor instructions

There are three types of coprocessor instructions:

Data-processing instructions These start a coprocessor-specific internal operation.

Data transfer instructions These transfer coprocessor data to or from memory. The address of the transfer is calculated by the ARM processor.

Register transfer instructions These allow a coprocessor value to be transferred to or from an ARM register.

4.0.9 Exception-generating instructions

Two types of instruction are designed to cause specific exceptions to occur.

Software interrupt instructions SWI instructions cause a software interrupt exception to occur. These are normally used to make calls to an operating system, to request an OS-defined service. The exception entry caused by a SWI instruction also changes to a privileged processor mode. This allows an unprivileged task to gain access to privileged functions, but only in ways permitted by the OS.

Software breakpoint instructions BKPT instructions cause an abort exception to occur. If suitable debugger software is installed on the abort vector, an abort exception generated in this fashion is treated as a breakpoint. If debug hardware is present in the system, it can instead treat a BKPT instruction directly as a breakpoint, preventing the abort exception from occurring.