High Performance Non-Planar Tri-gate Transistor Architecture

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What Are We Announcing?

- **Invention of a novel tri-gate fully depleted transistor with industry leading performance**
  - **Research targeted for 2nd half of the decade**
- **A three dimensional extension of the TeraHertz architecture**
  - **Highest reported drive current for non-planar devices**
  - **Depleted substrate improves I_{off} leakage**
- **Improved manufacturability over proposed double gate structures**
  - **Uses 300mm equipment and existing lithography capabilities**

Why is this Important?

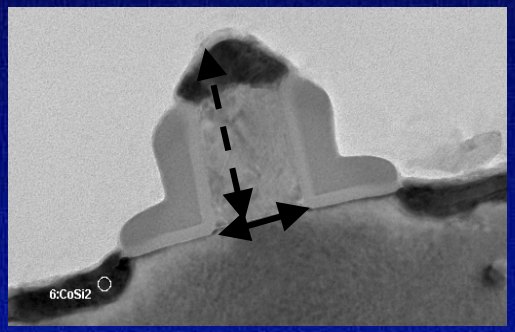
- **Transistor research breakthroughs will allow us to continue Moore's Law through end of decade**
- **IC Industry is making transition from Planar to Non-Planar Transistors**
- **This development has potential to enable products with higher performance that use less power**
- **Intel transistors lead industry performance in both research and manufacturing**
- **Intel's $4B investment in R&D continues on track: delivering a new process technology every 2 years**

Moore's Law
A new technology every 2 years

Process Name	P856	P858	Px60	P1262	P1264	P1266	P1268
1st Production	1997	1999	2001	2003	2005	2007	2009
Lithography	.25µm	.18µm	.13µm	90nm	65nm	45nm	32nm
Gate Length	.20µm	.13µm	<70nm	<50nm	<35nm	<25nm	<18nm
Wafer Size (mm)	200	200	200/300	300	300	300	300

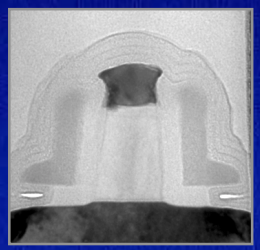
Accelerated Scaling of Planar Transistors

130nm Node



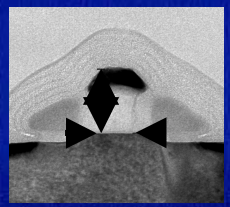
70nm Length (Production2001)

90nm Node



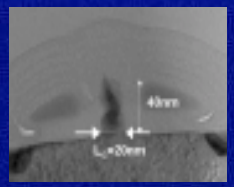
50nm Length (Production in 2003)

65nm Node



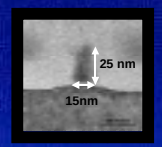
30nm Prototype (Production in 2005)

45nm Node



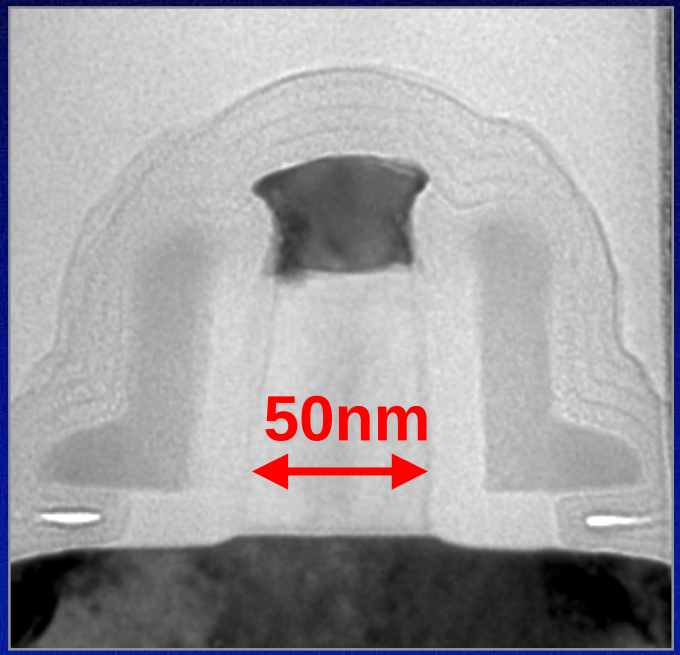
20nm Prototype (Production in 2007)

32nm Node



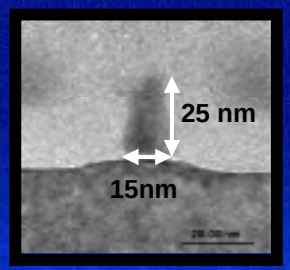
15nm Prototype (Production in 2009)

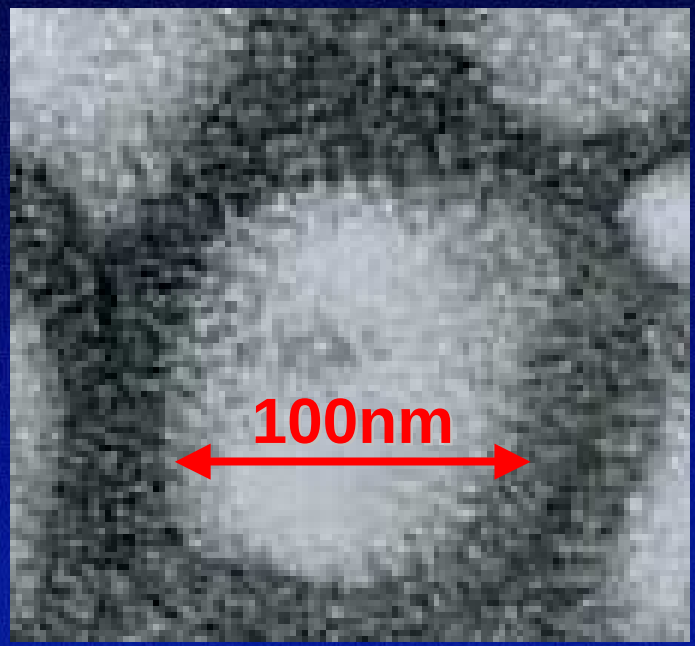
Silicon devices are Nanotechnology



Transistor for 90nm process

Source: Intel



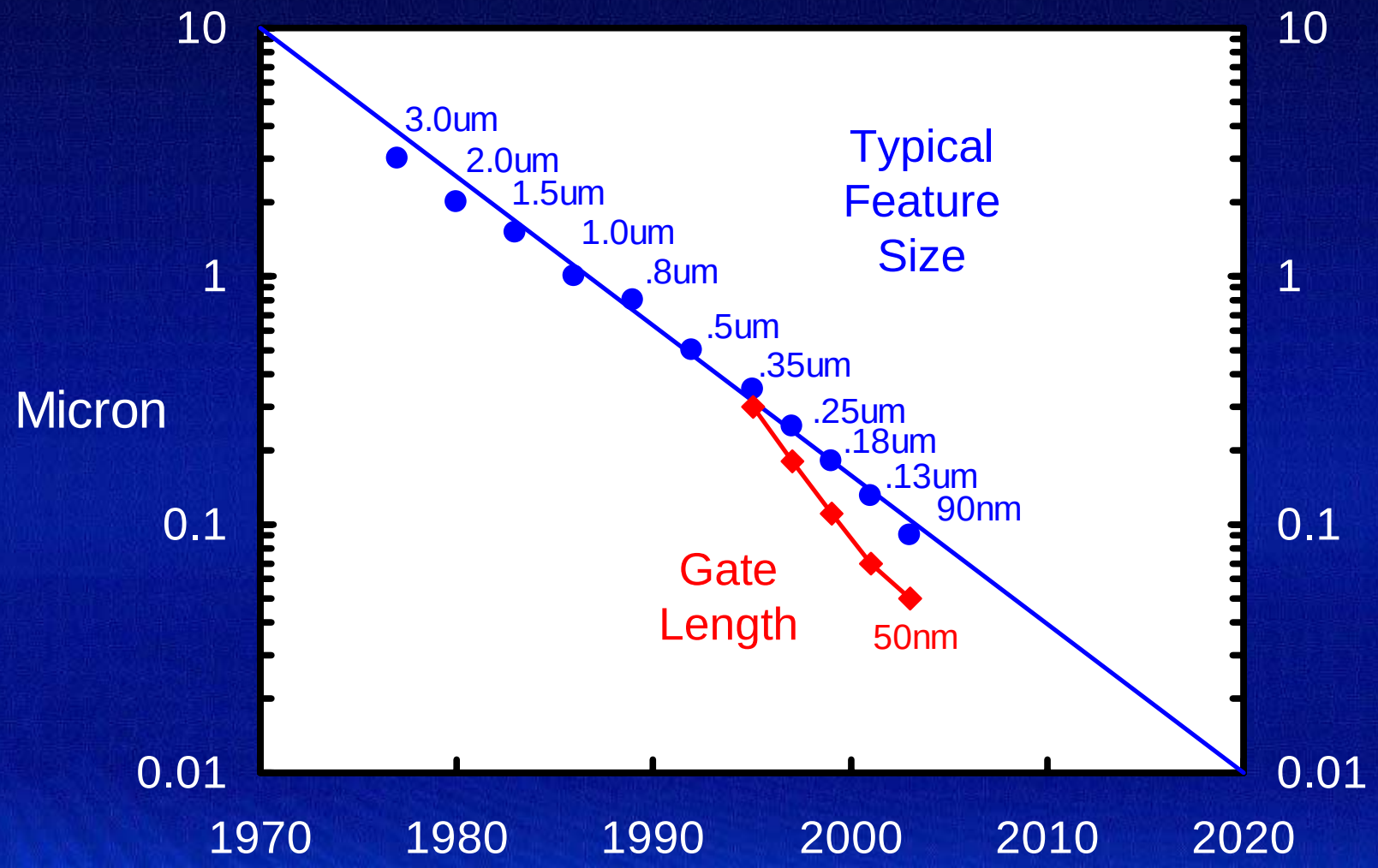


Influenza virus

Source: CDC

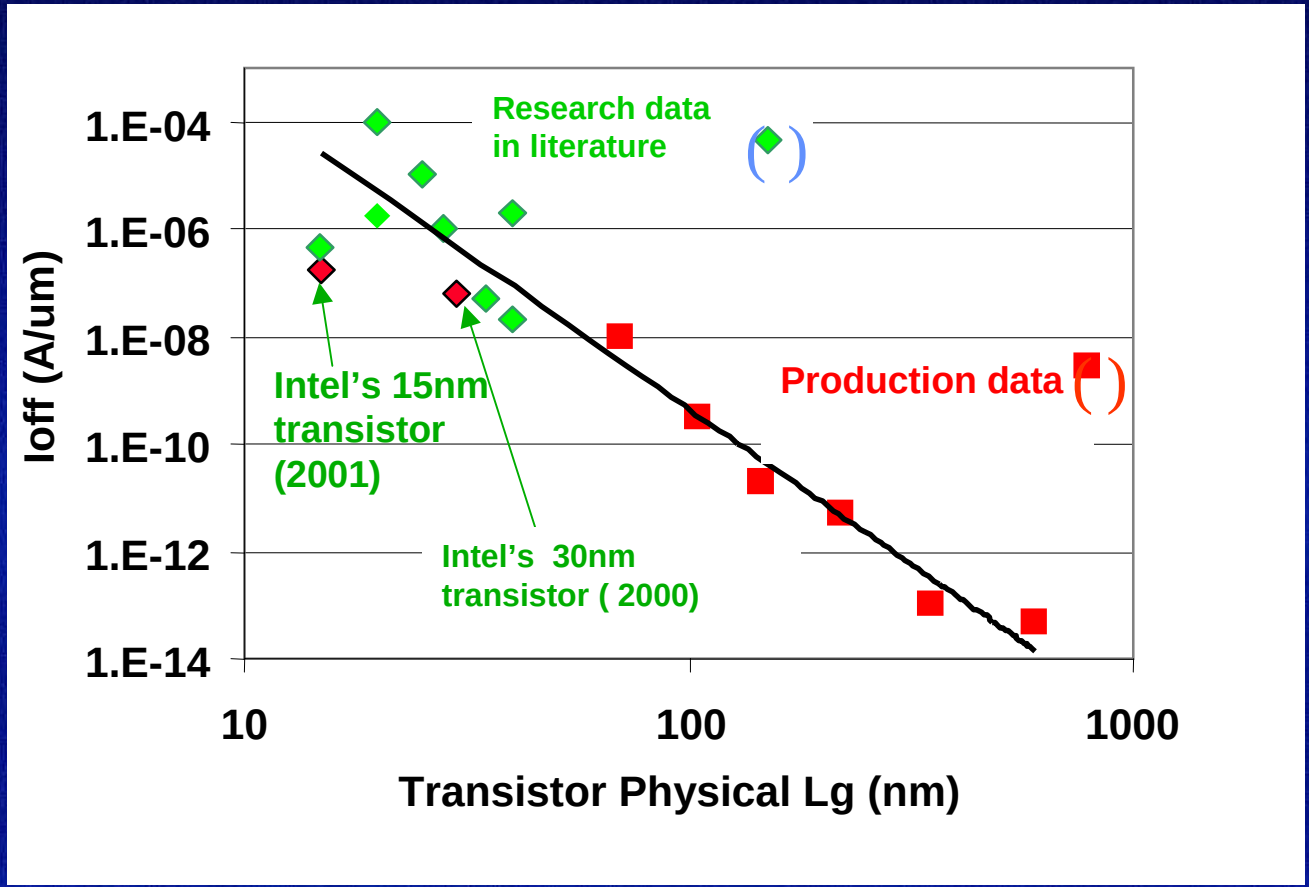
15nm Research Transistor

Transistor Gate Length Scaling



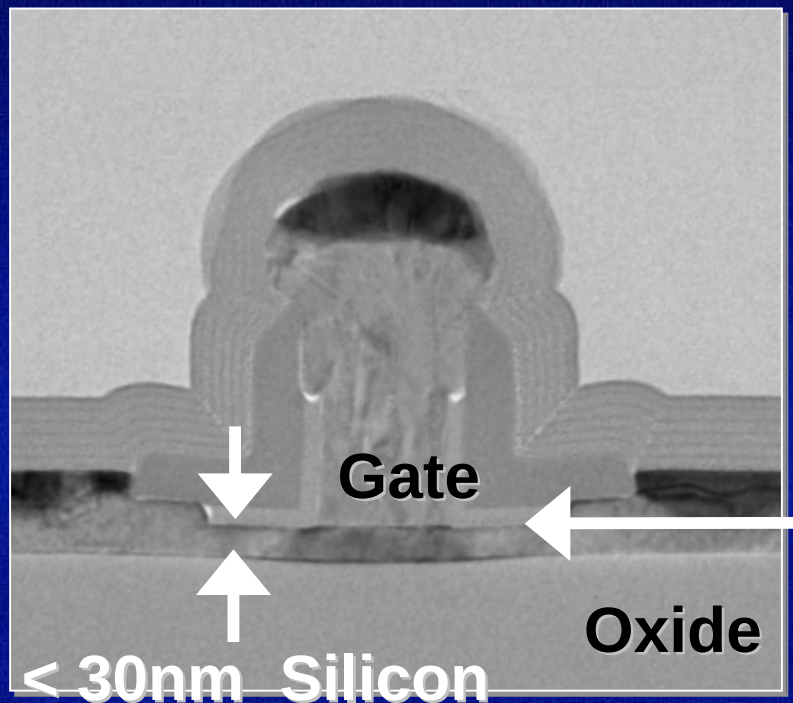
Transistor Gate Length is Smallest Feature on the Device

Planar Transistor Problem: Smaller Devices have Higher Leakage



We need novel device structures to meet this challenge

Intel's TeraHertz Transistor: Lower I_{off} Leakage

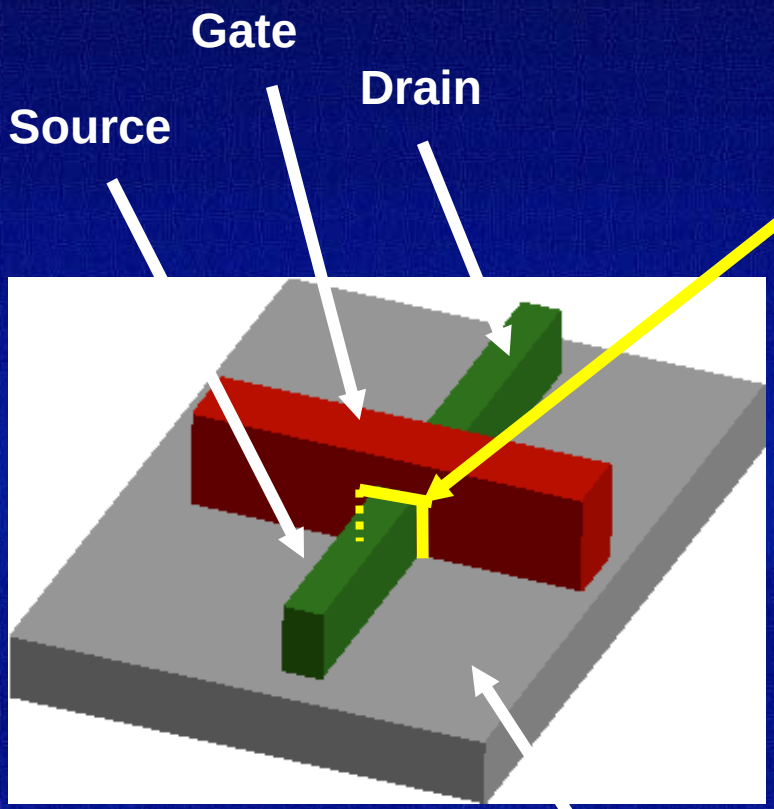


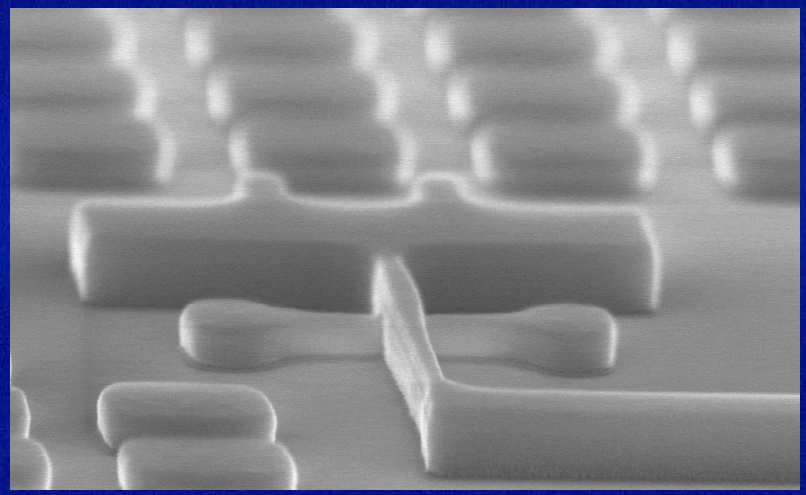
Fully Depleted Substrate: Subthreshold Leakage is Approaching Theoretical Minimum

A Switch to Non-Planar CMOS Transistors

- **Planar TeraHertz Transistor Improves Leakage**
  - **Control of Nano-thick Silicon Layer becomes the Manufacturing Issue**
- **Three Dimensional Devices (Non-Planar) have been Proposed by Researchers**
  - **Dual Gate, FinFET, etc.**
  - **Complex Fabrication processes**
  - **Measured Device Performance has been Disappointing**

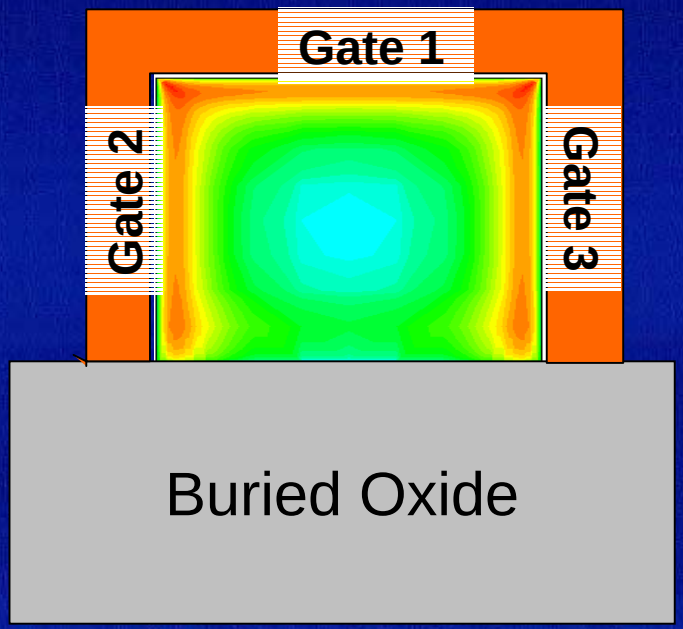
New Tri-Gate Transistor Structure



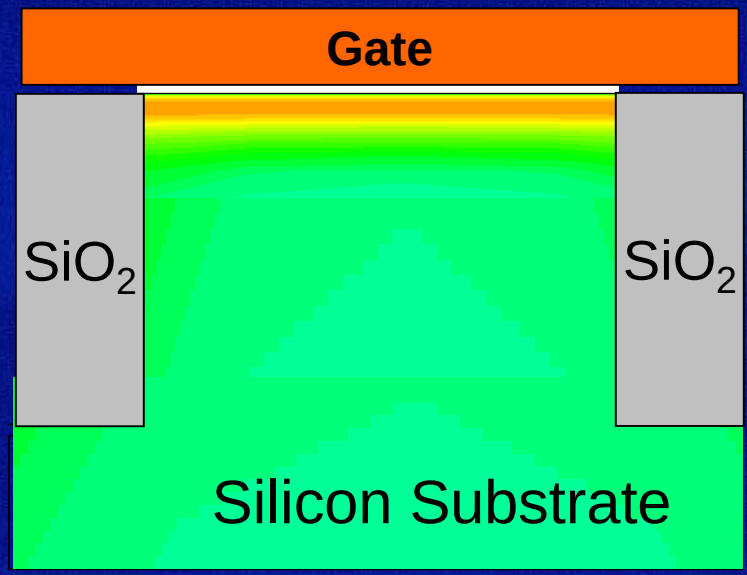


Tri-gate Transistor works in Three Dimensions

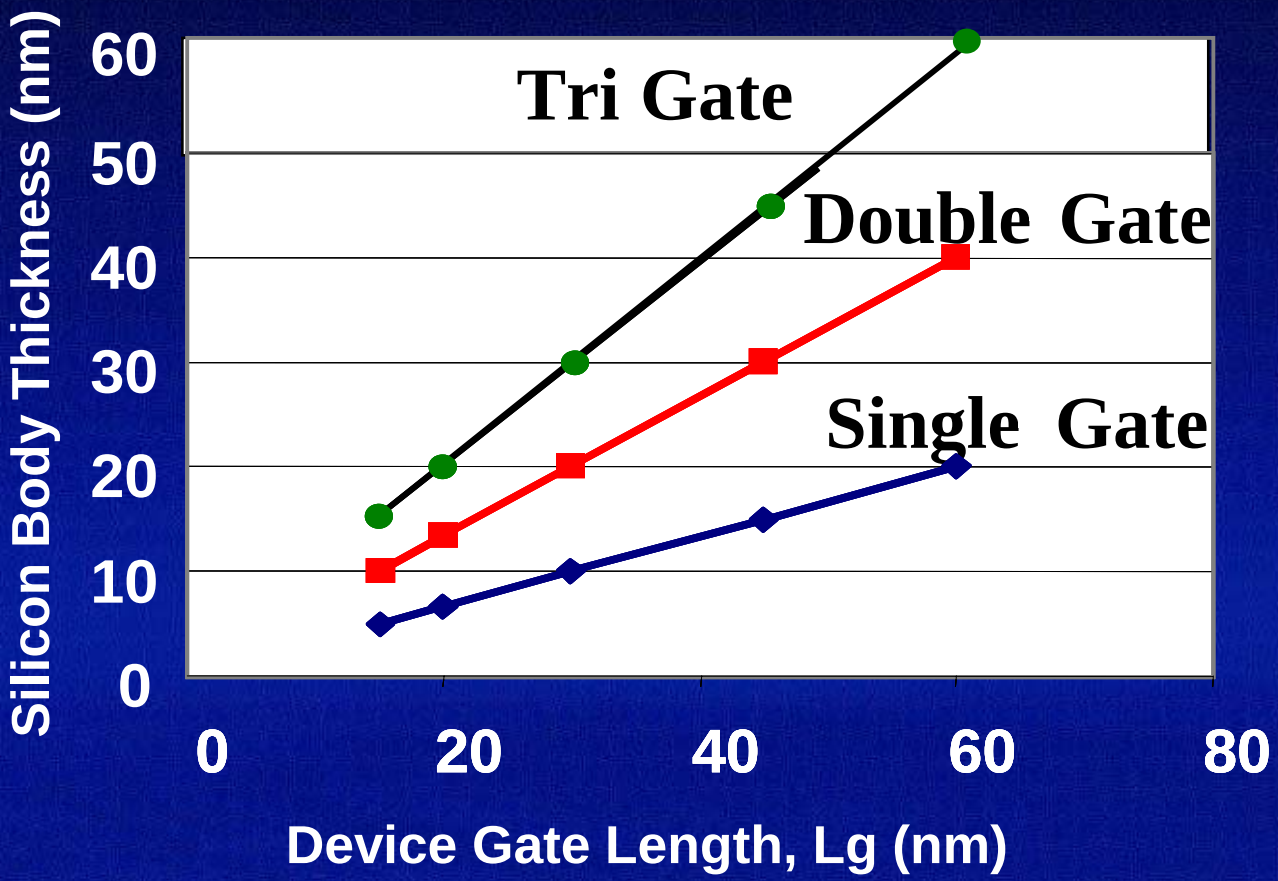
Tri-Gate



Planar CMOS

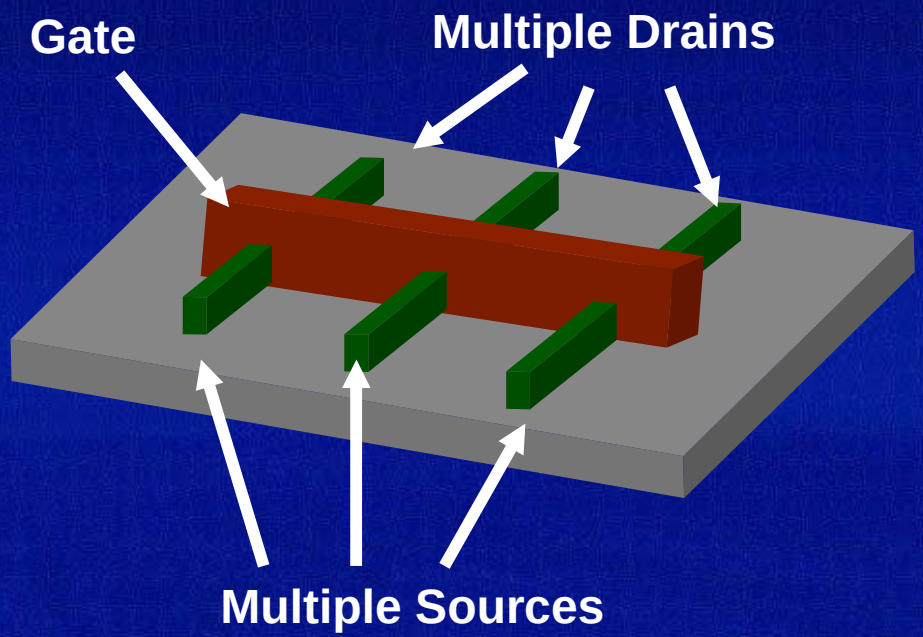


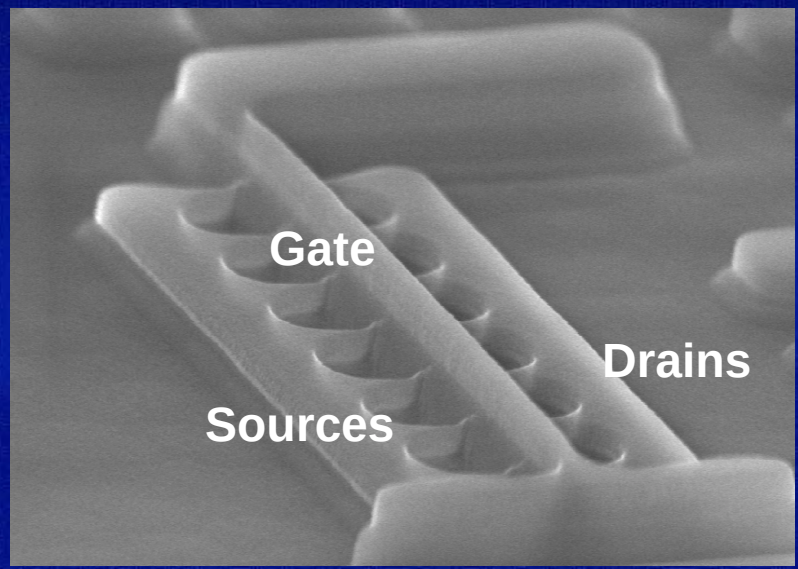
Tri-Gate's Geometry Advantage



Tri-gate is Fully Depleted Without Unusual Lithography Patterning or SOI Thickness Control Issues.

Multi-Channel Tri-gate Devices: Even More Drive Current





Conclusions

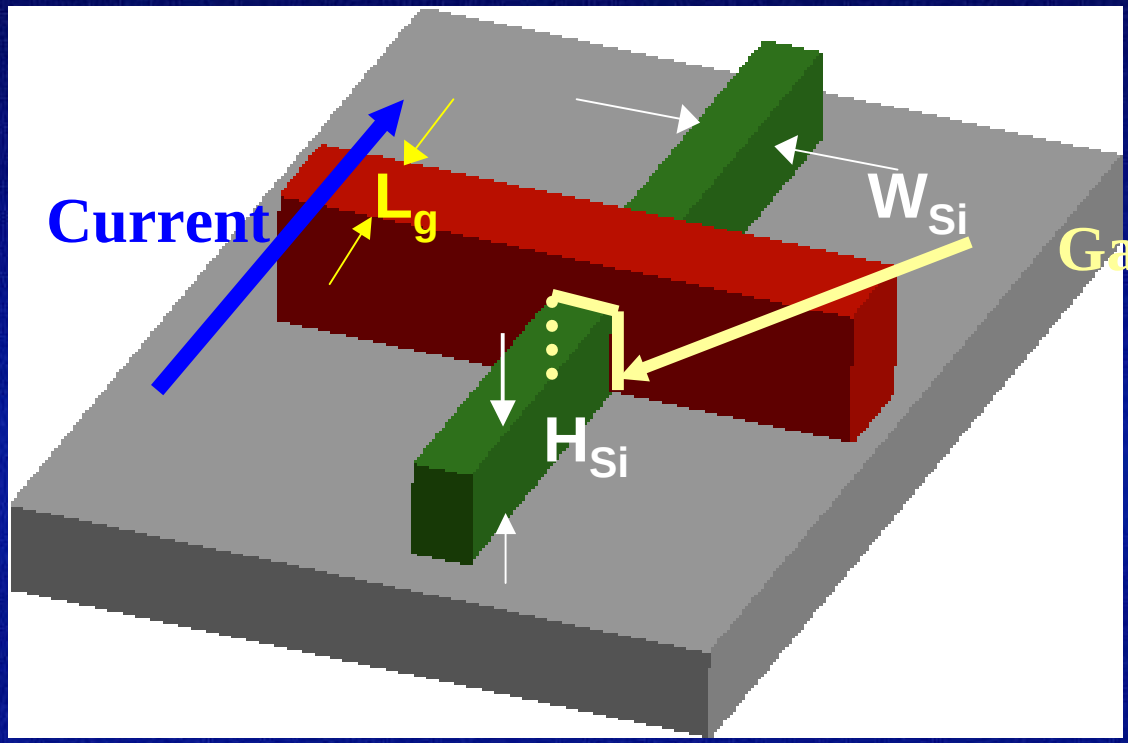
- **High-Performance Tri-Gate Fully-Depleted CMOS with 60nm physical gate length has been Demonstrated**
- **Tri-gate Fully-Depleted CMOS exhibits lower leakage than standard planar CMOS**
  - **Similar to Planar TeraHertz Transistor**
- **Unique Tri-Gate Geometry is more Manufacturable than Fully-Depleted Planar and Double Gate structures.**
- **Tri-gate with Spacer-Defined Fins has Potential to deliver 20% Higher Total Current per unit Layout Area than Standard CMOS**

Additional details of this Tri-gate transistor technology will be presented at the International Solid State Device and Materials Conference in Nagoya Japan on Sept 17, 2002

For further information on Intel's silicon technology, please visit the Silicon Showcase at www.intel.com/research/silicon

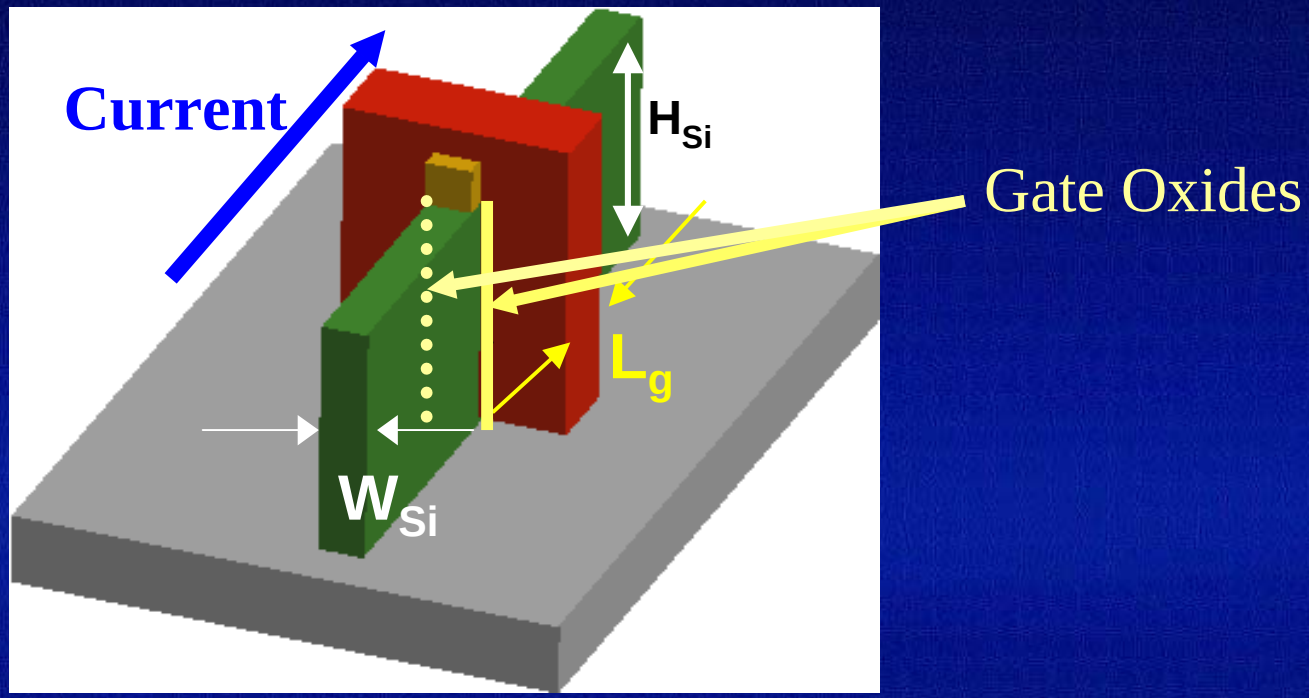
BACK – UP MATERIAL

New Tri-gate Transistor Structure



Improved Manufacturability
Width = Height = Gate Length

Double Gate FinFET Transistor



Major Problem: Fin Width must be Narrower than Gate Length
Lithography becomes the Key Limiter

New materials Extend Performance of 90nm Planar Transistors

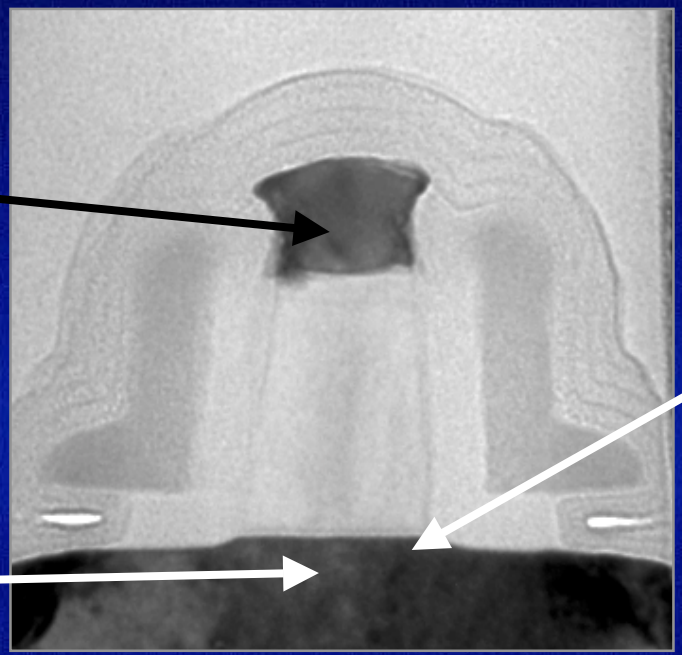
Changes made

Gate

Silicide added

Channel

Strained silicon



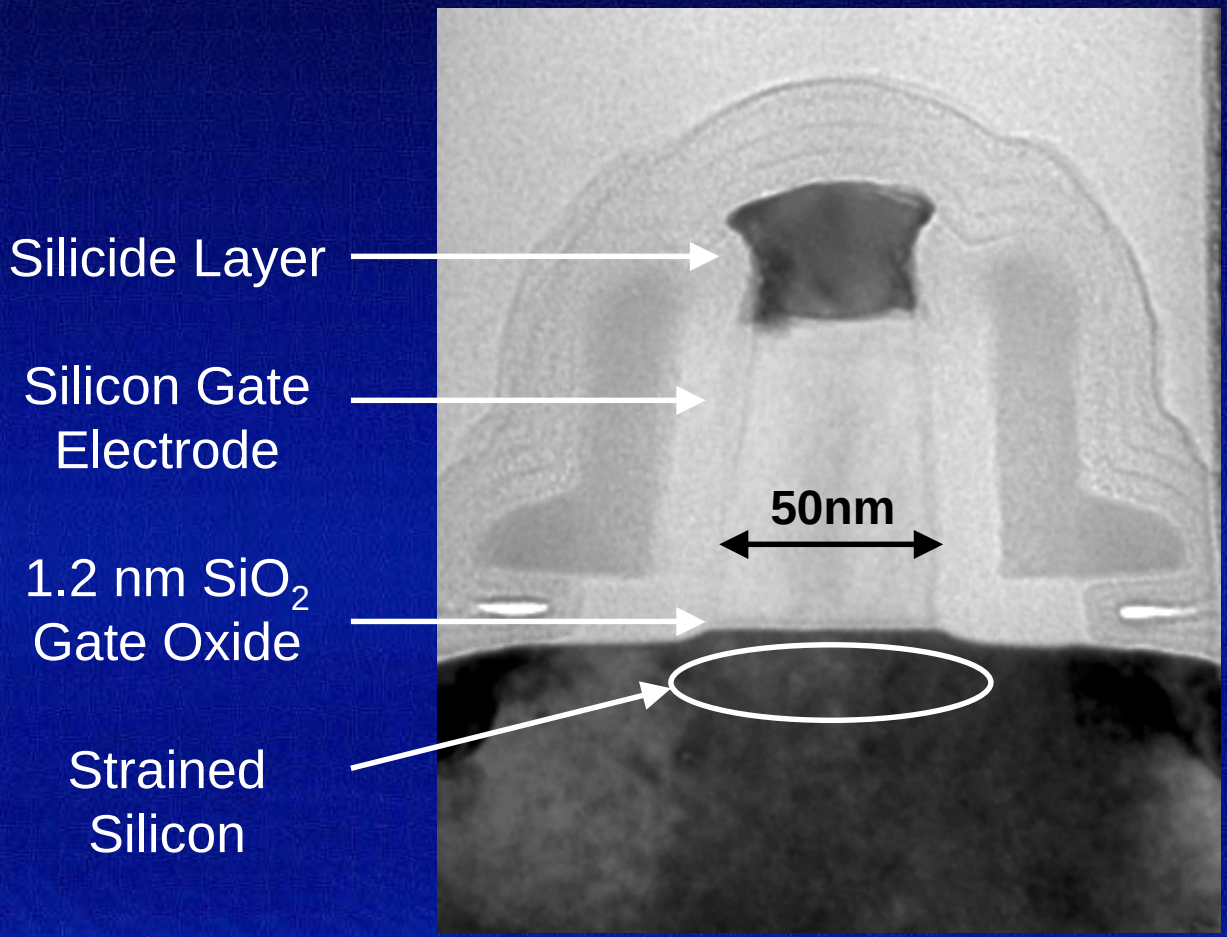
Transistor

Future options

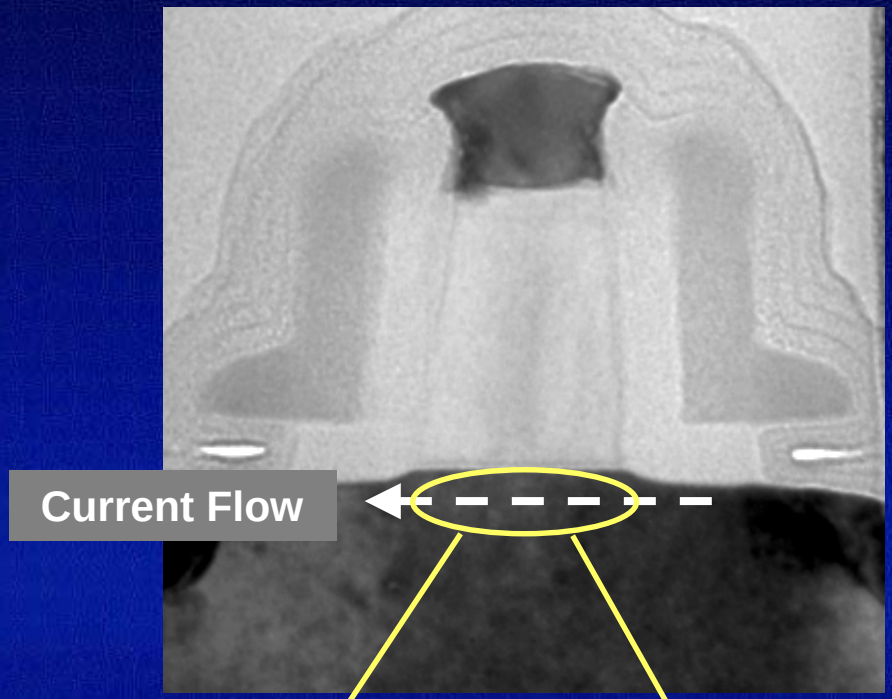
High-k gate dielectric

New transistor structure

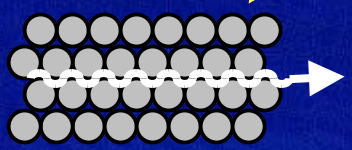
90 nm Generation Transistor

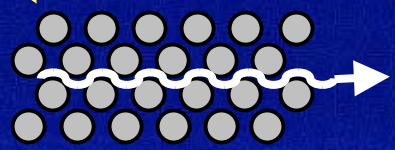


Strained Silicon Transistors



Normal electron flow





Faster electron flow

Normal Silicon Lattice **Strained Silicon Lattice**