Investigation about practical design techniques to mitigate Vt variability in NAND FLASH memories

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MISSION

Investigate practical design techniques to mitigate Vt variability in NAND FLASH memories

Practical= *Compatible with read/program device performance*

Design= *Focus on design software/hardware techniques and not on process/physical mechanism*

Vt Variability= *Different Vt string values obtained at different read times (including RTS phenomena)*

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PLAN

- **Basic RTS Theory**
- **Vt variability in NAND FLASH Memories (RTS, Cycling, Baking at 90nm and 35nm)**
- **Investigation about preconditioning techniques to mitigate Vt variability in NAND FLASH memories (35nm)**

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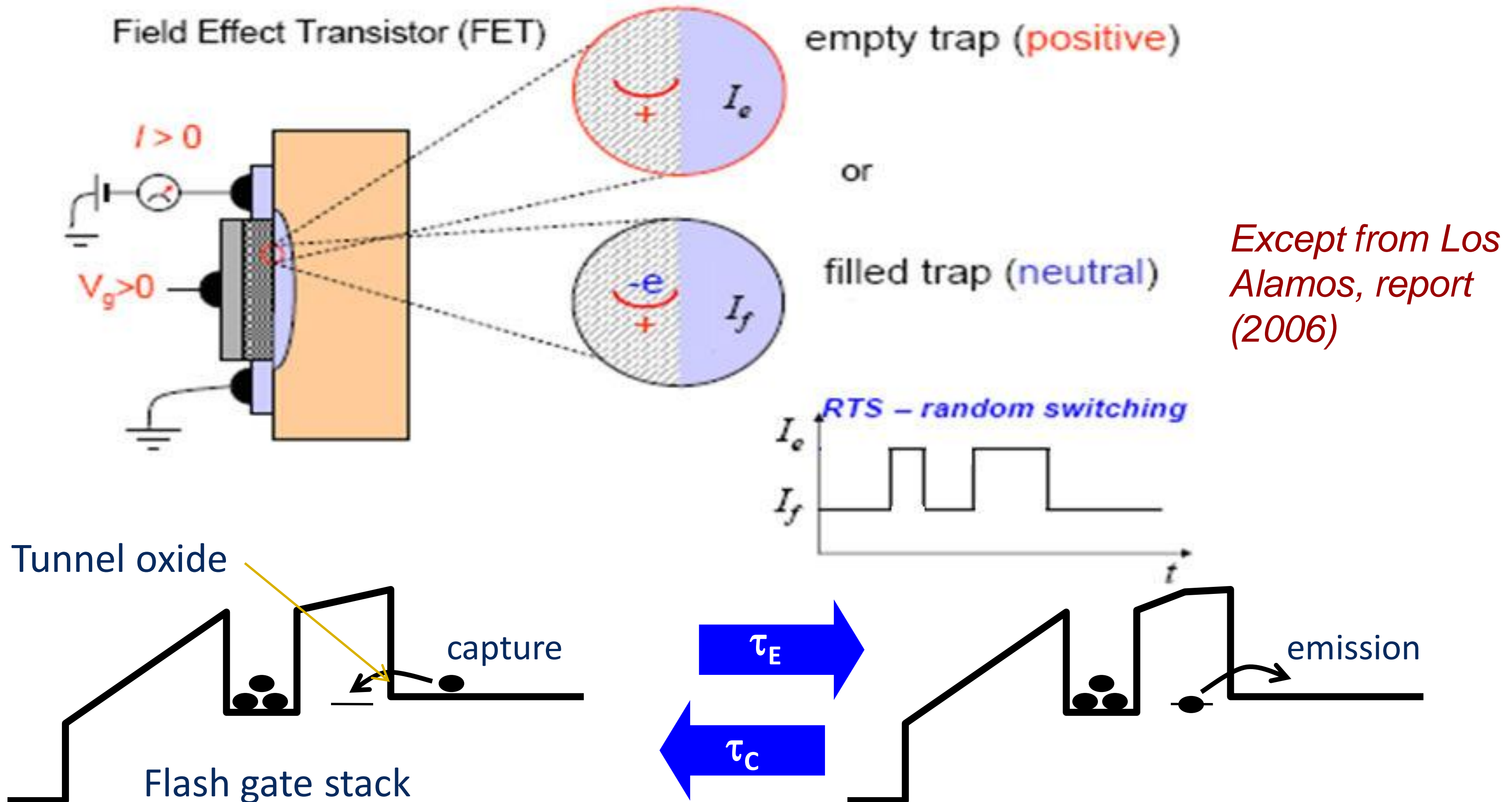
Basic RTS Theory
RTS (Random Telegraph Signal)

- **Drain current fluctuation due to trapping and detrapping of channel electron at the defect ($|E_F - E_{trap}| < kT$) at SiO_2 and SiO_2/Si interface**
- **Drain current fluctuation is due to number of carrier fluctuation and mobility**



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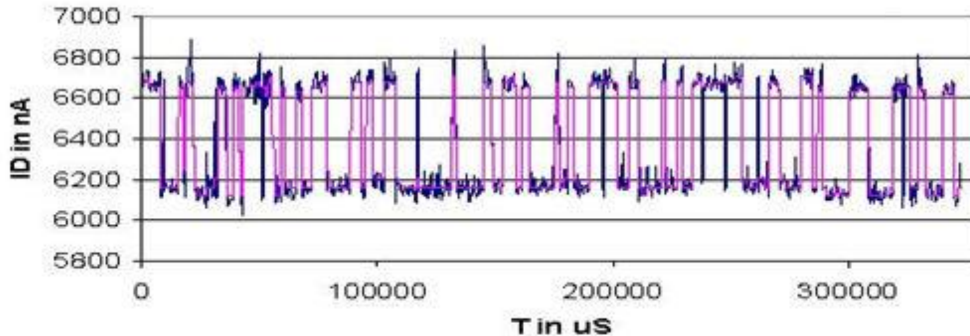
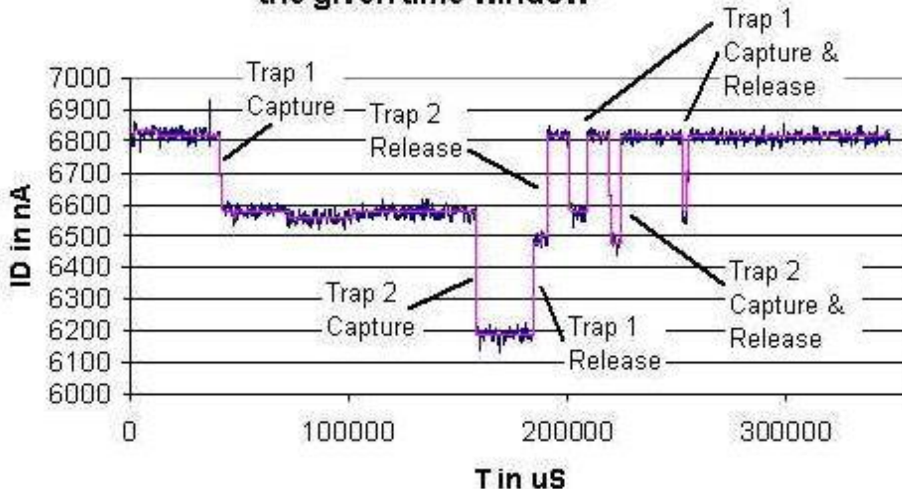
Basic RTS Theory
Time domain Behavior



-Drain current makes clear transitions between two levels, that develops on µs-ms time range.

-There is other noise superimposed on the discrete levels but clearly there are two identifiable discrete levels at which the current is stable for some random amount of time



-Some cells exhibit multiple levels.

-There are 4 discernable individual levels, presumably the result of two separate traps operating independently, in the example on the left

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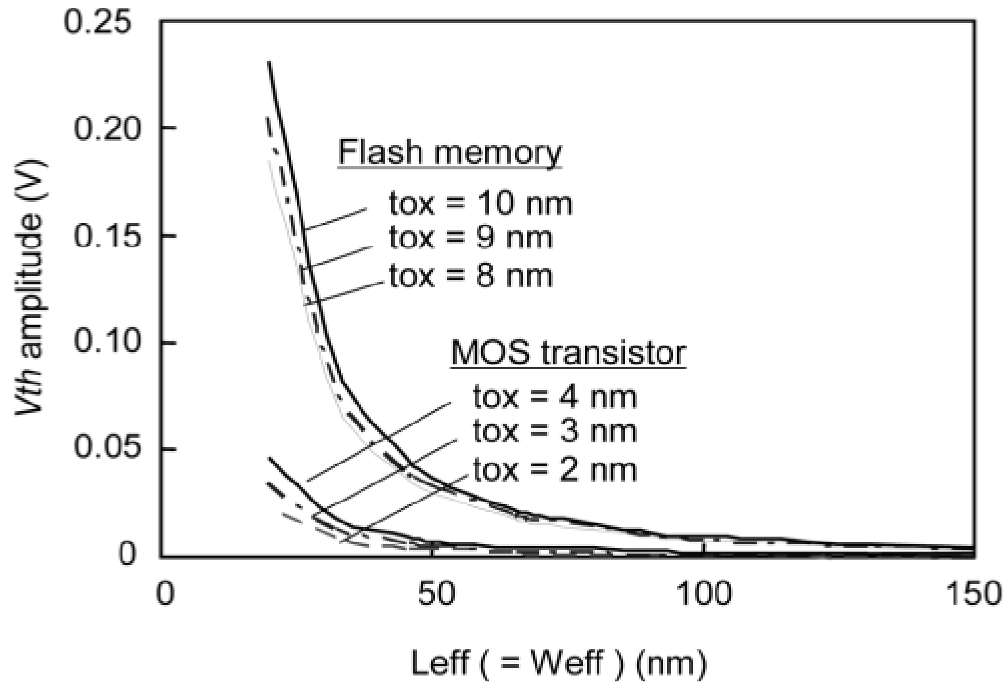
Basic RTS Theory
RTS and scaling issues



Kurata ,et al, IEEE journal of solid-state circuitsVol.42, (June 2007)

-RTS effect is increasing with MOS device scaling

- The traps number in the channel is reducing , but their weight Vs Area is growing up with scaling

$$\Delta V_{t\ by\ RTS} \approx \frac{q}{L_{eff} \cdot W_{eff} \cdot C_{ox} \cdot GCR}$$

Flash Memories are particularly subjected to RTS (for same area) for 3 main reasons:

-The oxide thickness t_{ox} is thicker than transistor

-The coupling factor **GCR** make worse RTS effect

-Flash are analog devices (mlc devices)

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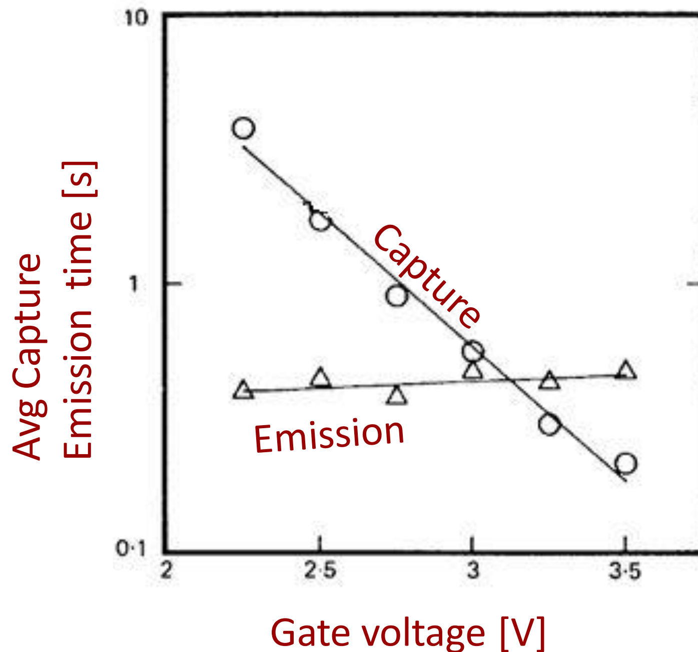
Basic RTS Theory
RTS is a strong function of V_{Gate}

Avg capture & emission time



- Emission and Capture are associated to different physical mechanism
- Emission is more sensitive to activation energy ,while capture to mean cross section

Kirton (1989)

Capturing process is a strong function of V_G : V_G ↑ →avg τ_c↓ (easily captured)

Emission process is a weak function of V_G : V_G ↑ → a little change in avg τ_e

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Vt variability in Nand Flash Memories
Experiments conditions

Environment setup is based on a board connected to a Pc using parallel port, more sophisticated equipment were not used not available full time

All data sensing were performed using internal sensamp circuits and routines

A single threshold measure is a threshold distribution based on a data set composed
By several thousands Bit Lines (BL) belonging to the same Word Line (WL).

The Word Line evaluated has been selected in the middle of NAND string to avoid edge effects.

All the cells belonging to the selected Word Line are programmed in the range of 1V

All the cells belonging to non selected Word Lines are erased
(their Vt is usually less than -2V).

We evaluated ΔVts of a word line due RTS over 3500 consecutive threshold measures
Each measure need almost 6 seconds to be performed

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Vt variability in Nand Flash Memories

Vt Search in one page

BL0 BL1 …BLn

selected WL

sensing

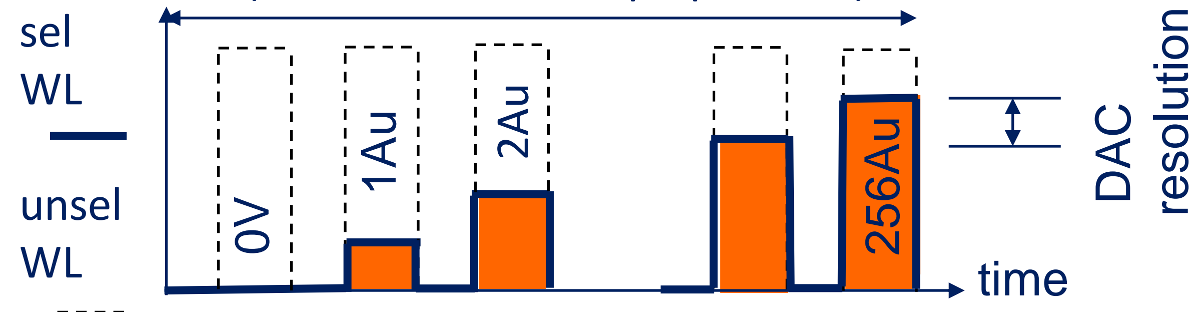
bytemux

dout(8)

array to sensing parallel download

sensing to out serial transfer

6 sec (PC evaluation + chip operation)



At each WL step :

1) array to sens download
2) byte mux
3) if bit flips from 0 to 1 the WL value is stored as cell VT.

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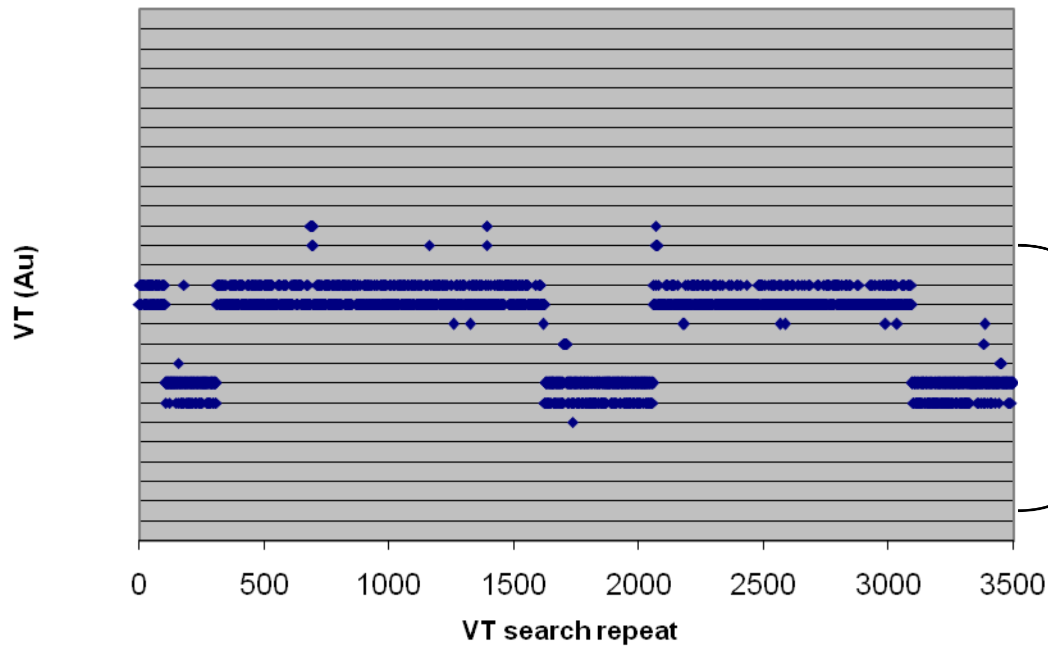
Vt variability in Nand Flash Memories

Multimodal detection (RTS)



Number of measures having specific VT		Data filtered at 15% max VT value
11		0
12		0
0		0
623		623
1800		1800
10	bimode criteria	0
16		0
4		0
720		720
253		0
1		0

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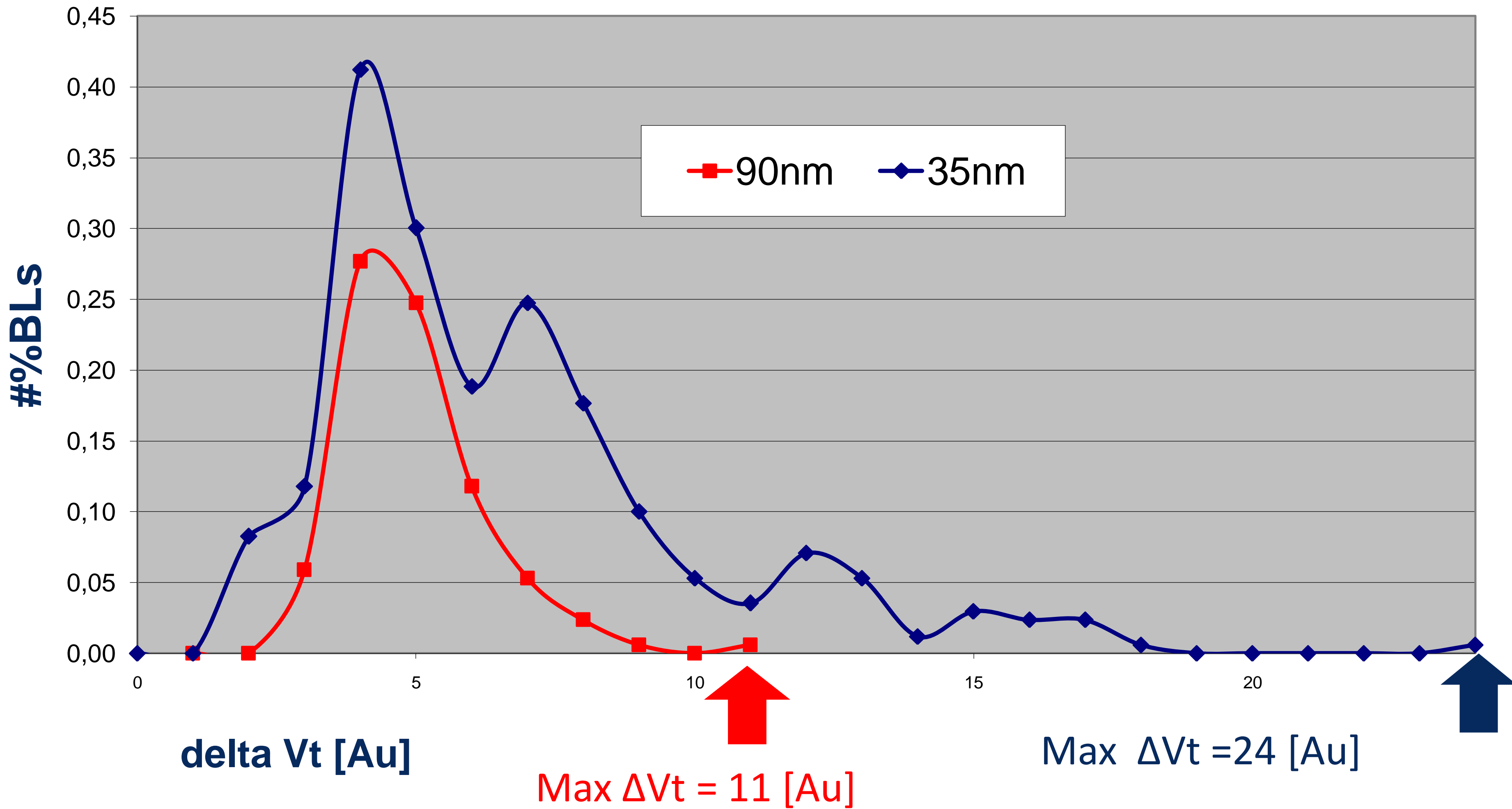
Vt variability in Nand Flash Memories
RTS 90 nm and 35nm



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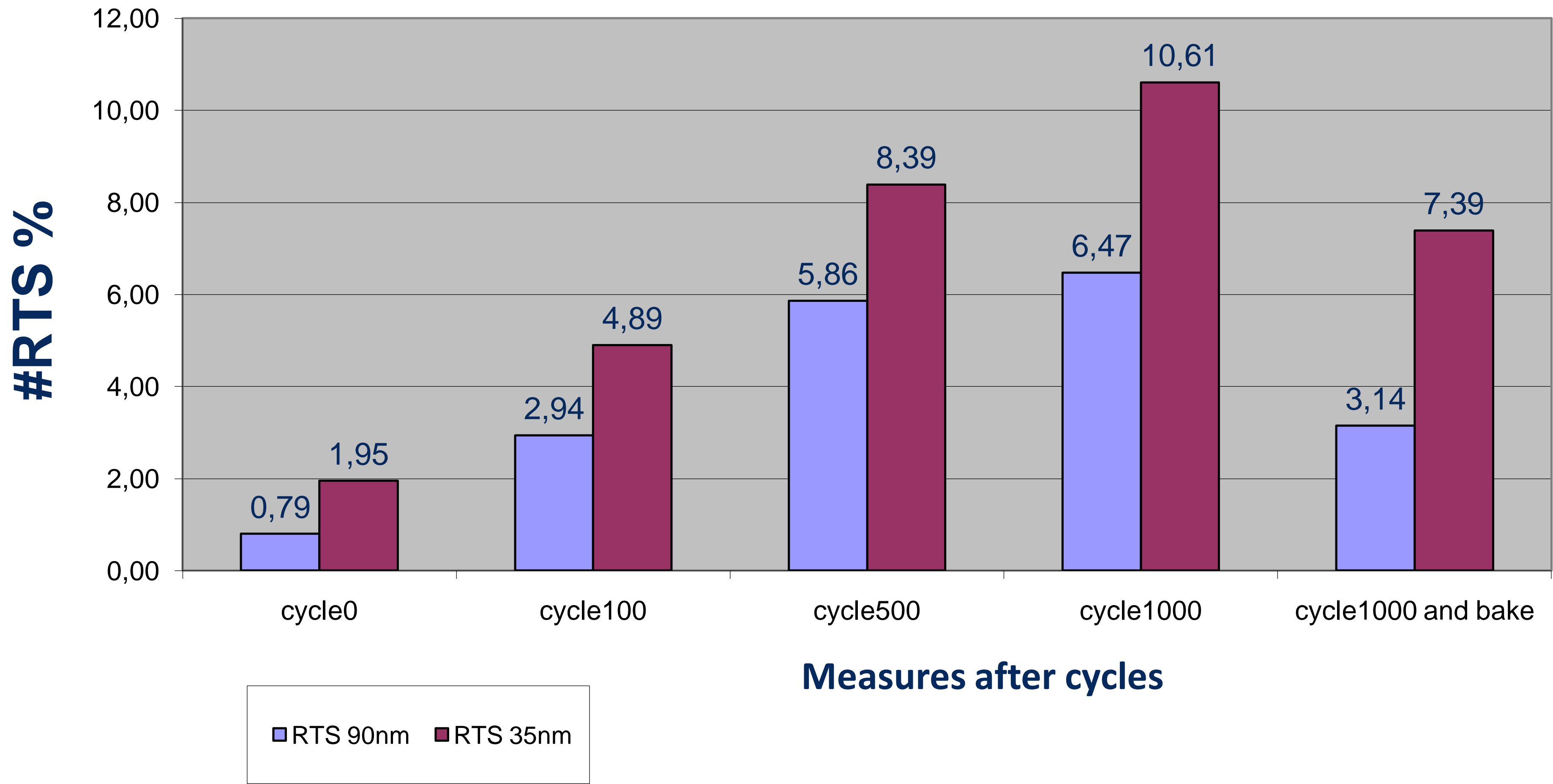
Vt variability in Nand Flash Memories
RTS 90 nm and 35nm



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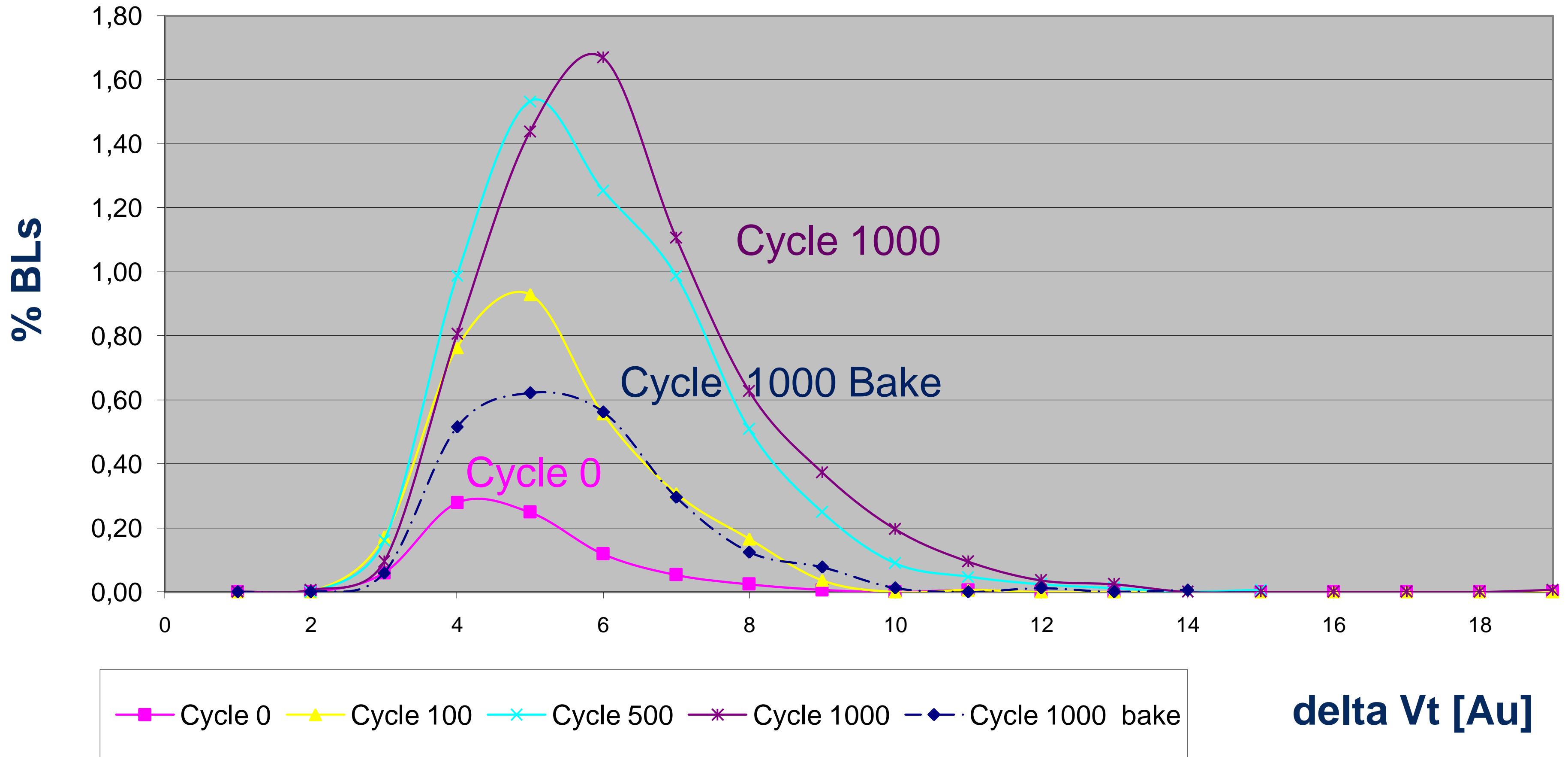
Vt variability in Nand Flash Memories

90nm RTS vs delta VT with cycling/baking



Max delta Vt value of BLs with bimodal behavior and their number increase with cycling

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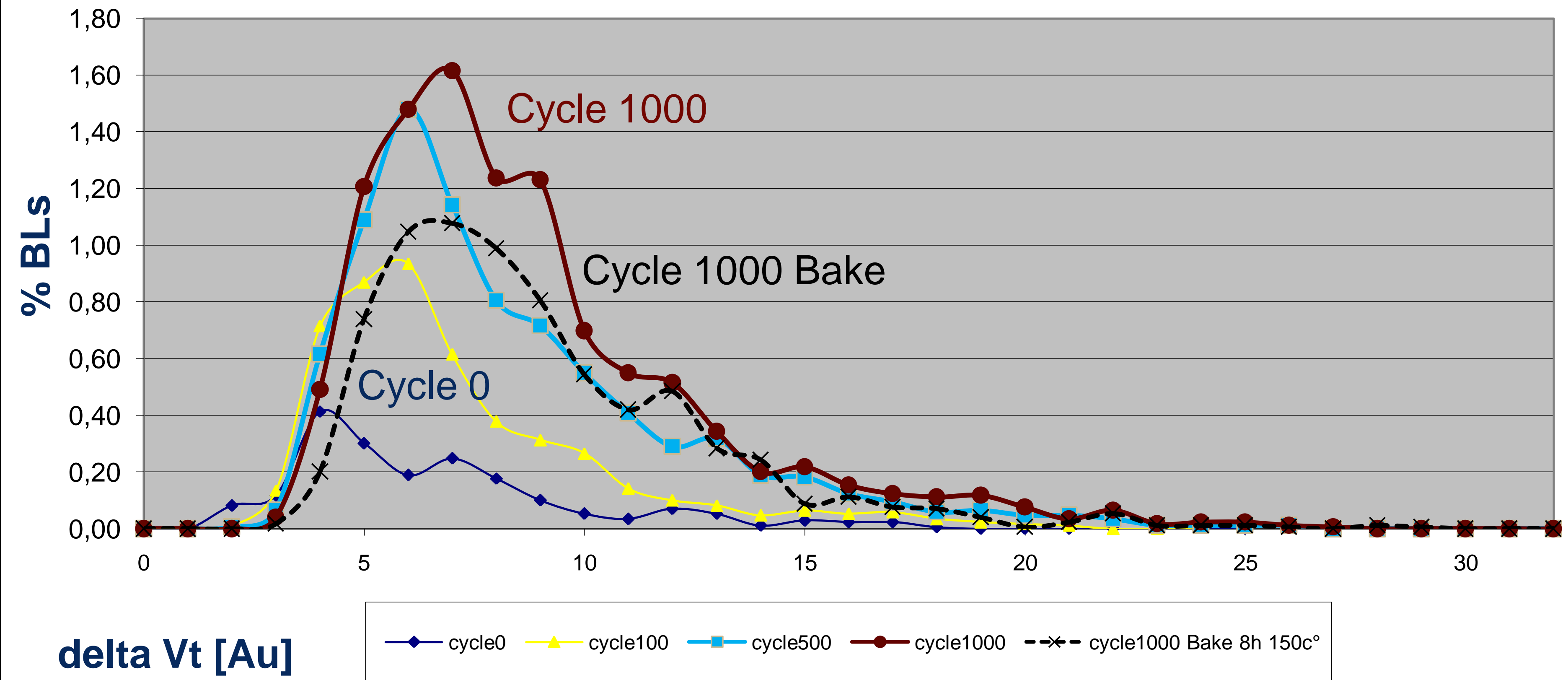
Vt variability in Nand Flash Memories
35nm RTS with cycling/baking



Max delta Vt of BLs with bimodal behavior and their number increase with cycling

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Precondition Concept

The concept of preconditioning is to apply an electrical field through the string channel before any read (or program verify) operation.

The basic idea of the electrical field is to fill up the traps and perform the subsequent read in a time frame less then the time needed to detrap.

Electrical field is applied using word lines voltages that can be steady (biasing) or toggling (agitation).

The channel can be biased through the Bit Lines (channel ON) or left free to boost (channel OFF).

Useful references dealing of preconditioning techniques in different flavors are :

1) Mokhlesi et al. “Noise reduction technique for transistors and small devices utilizing an episodic agitation”.
   US patent 7,092,292 (Sundisk)
2) Compagnoni et al. “Statistical Investigation of Random Telegraph Noise ID instabilities at Different Initial Trap Filling Conditions”.
   IEEE 45th Annual International Reliability Physics Symposium.
   Phoenix 2007. Pags. 161-166.

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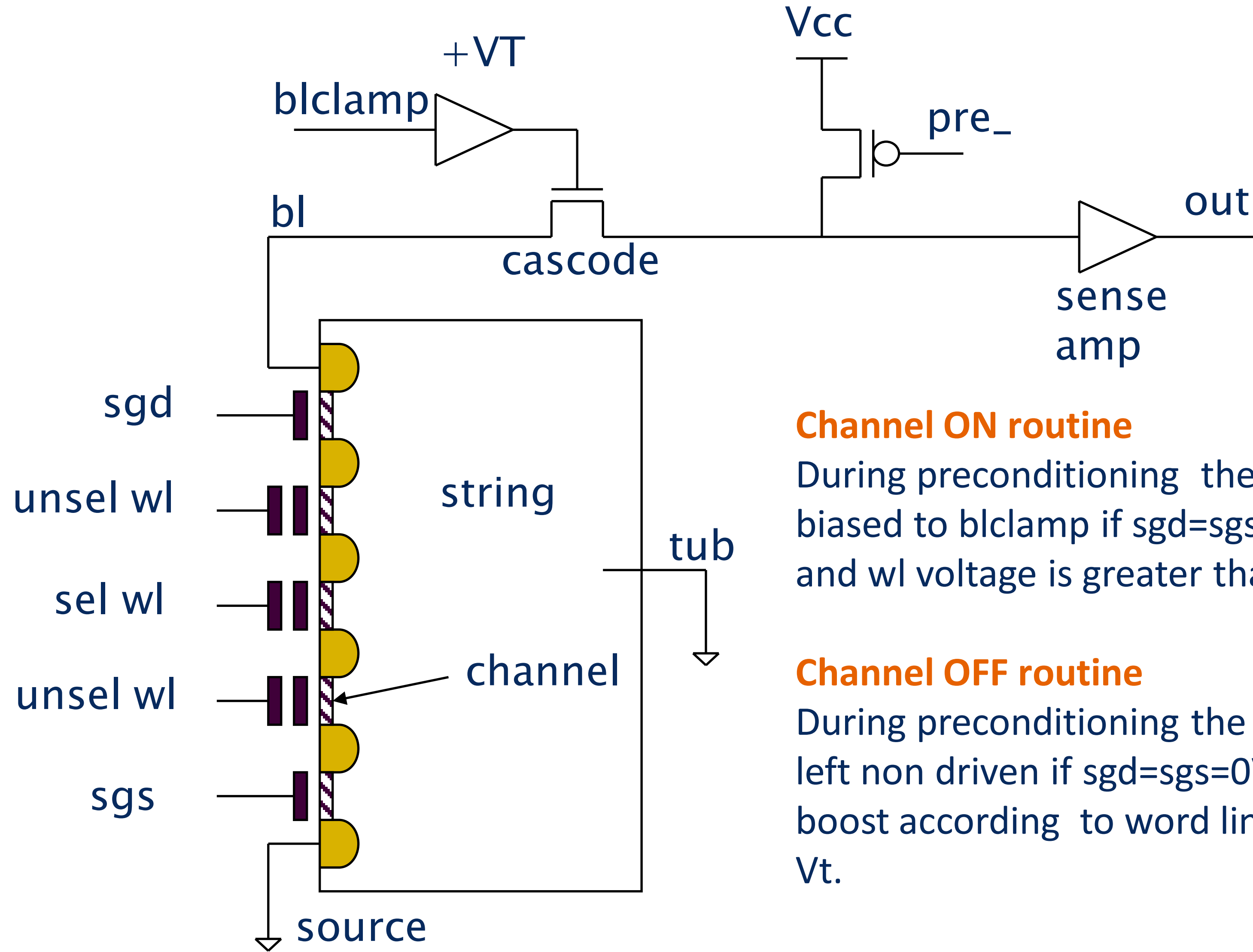
Precondition Concept



Channel ON routine

During preconditioning the channel can be biased to blclamp if sgd=sgs>2V and wl voltage is greater than cell V

Channel OFF routine

During preconditioning the channel can be left non driven if sgd=sgs=0V and free to boost according to word lines voltages and Vt.

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Vt search in one page with preconditioning

BL0 BL1 …BLn

selected WL

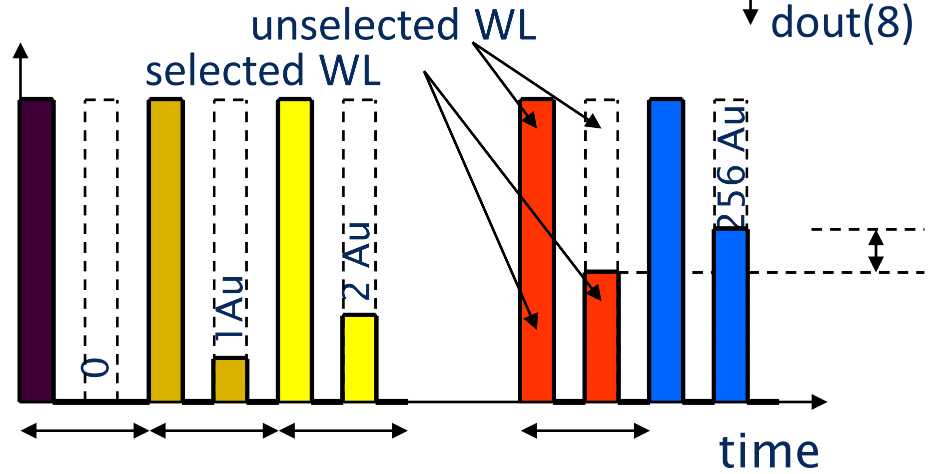
sensing

bytemux

dout(8)

array to sensing (parallel download)

sensing to out (serial transfer)



DAC resolution

At each WL step :

1) array to sens download
2) byte mux
3) if bit flips from 0 to 1 the WL value is stored as cell VT.

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Mitigation of Vt variability using preconditioning

Preconditioning experiments were performed on the same block.
Every time the block was erased and the selected WL programmed ;
RTS reference (normal Vt search) was taken before each precondition attempt;
After each Reference-Precondition, the selected WL was erased and programmed again

First results of the experiments using channel ON and OFF steady preconditioning at several pulse width and different voltage values of 0V ; 5V were suspicious because :

1) All the techniques gave almost equivalent mitigation effects of 50%.

2) Reference number of RTS taken before any precondition experiment were less than what usually seen taking a reference in a fresh block (block not checked at least in two months). We have met the same behavior in several different blocks

3) Preconditioning at 0V have the same mitigation effects of preconditioning at higher voltages.

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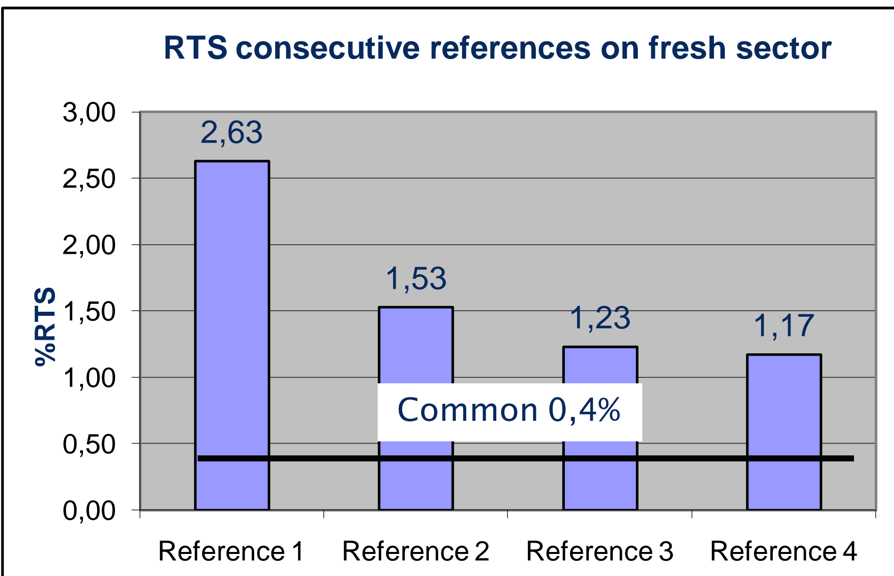
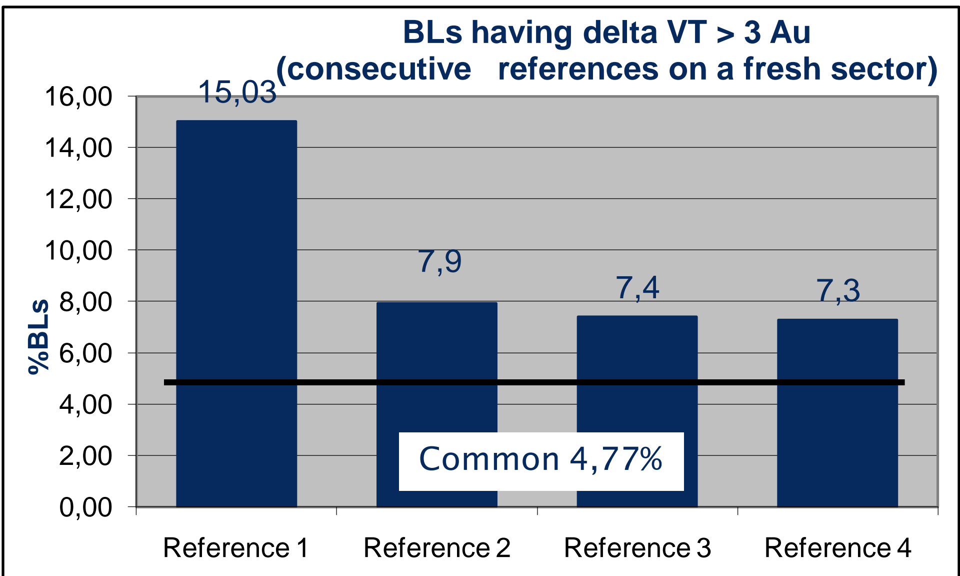
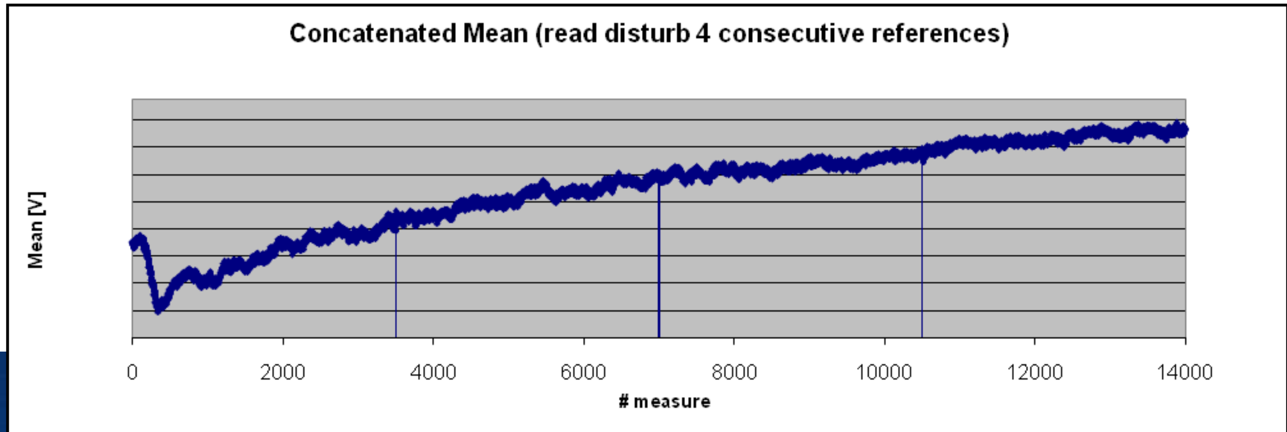
Sanity check in reference operation

Reference operation was suspected to perform an RTS mitigation.
To confirm this hypothesis, 4 consecutive references (each one composed by 3500 Vt search) were performed on a fresh sector with the following results :







1Au Intercept
Read disturb

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Conclusions

1) A common detection technique was applied to 90nm and 35nm RTS investigation in the same conditions

2) Software needed to data evaluation was developed

3) RTS versus Cycling-baking was evaluated at both technology nodes.

4) Firmware to implement precondition techniques (Channel ON/OFF) to mitigate RTS was written

5) Precondition experiments were performed at 35nm node

6) During preconditioning experiments has been noted that the Vt searching itself has a mitigation effect

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Future developments

1) Evaluate how and why Vt Searching has RTS mitigation effect (toggle and continuous ramp)

2) Evaluate back-pattern impact on RTS mitigation.

3) Evaluation and Preconditioning of “hard” RTS

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