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(54) **BACKGROUND BLOCK ERASE CHECK FOR FLASH MEMORIES**

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(58) **Field of Classification Search** ..... 714/716, 714/42, 43, 36, 48, 702, 718, 768, 7, 710; 710/52; 365/185.29, 185.08

See application file for complete search history.

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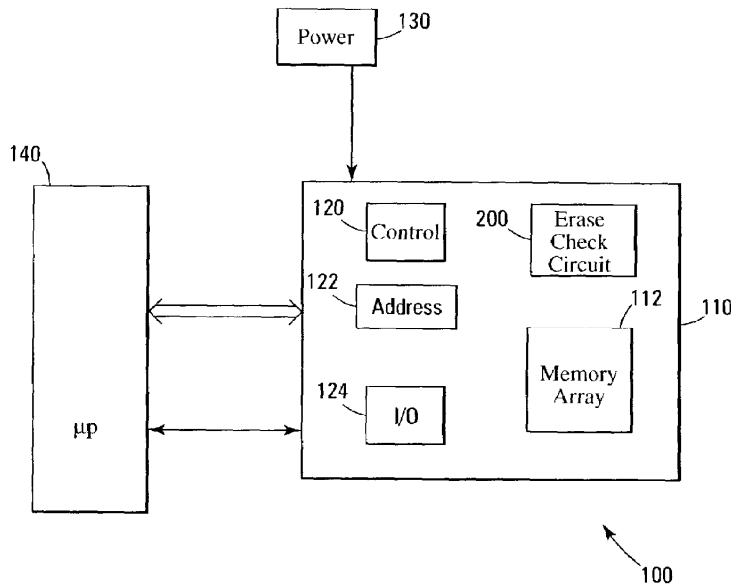
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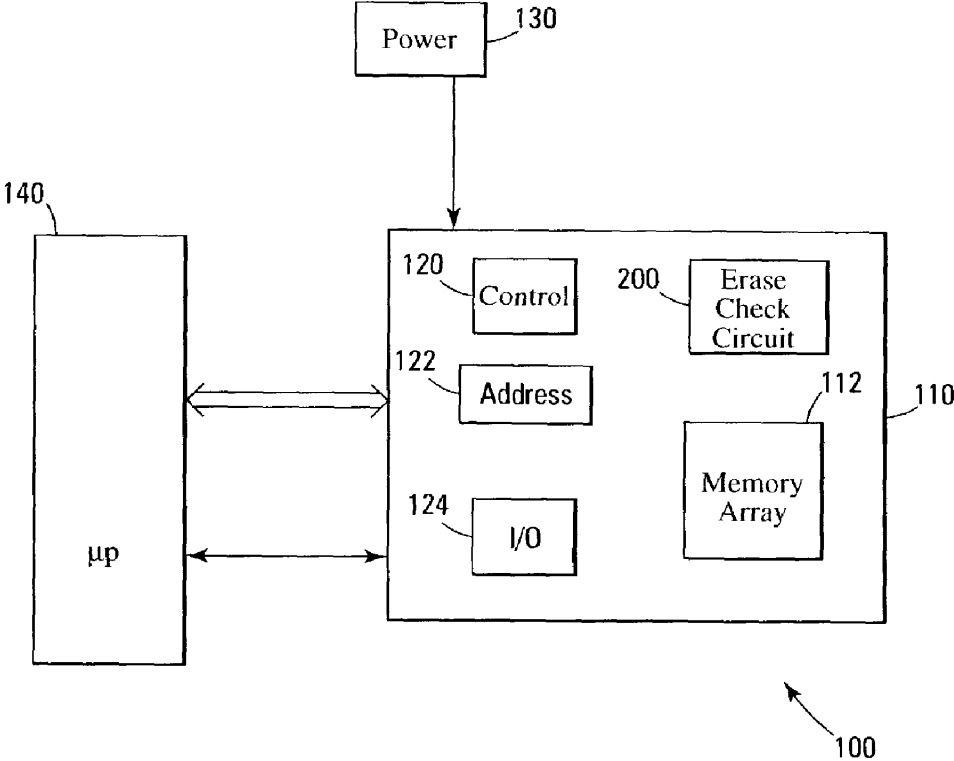
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(57) **ABSTRACT**

A flash memory erase check circuit is disclosed. One embodiment includes an on-chip circuit that quickly and reliably checks that the flash memory chip is actually erased even after data gain that has resulted, for example, from a long period of storage.

**36 Claims, 4 Drawing Sheets**





*Fig. 1*

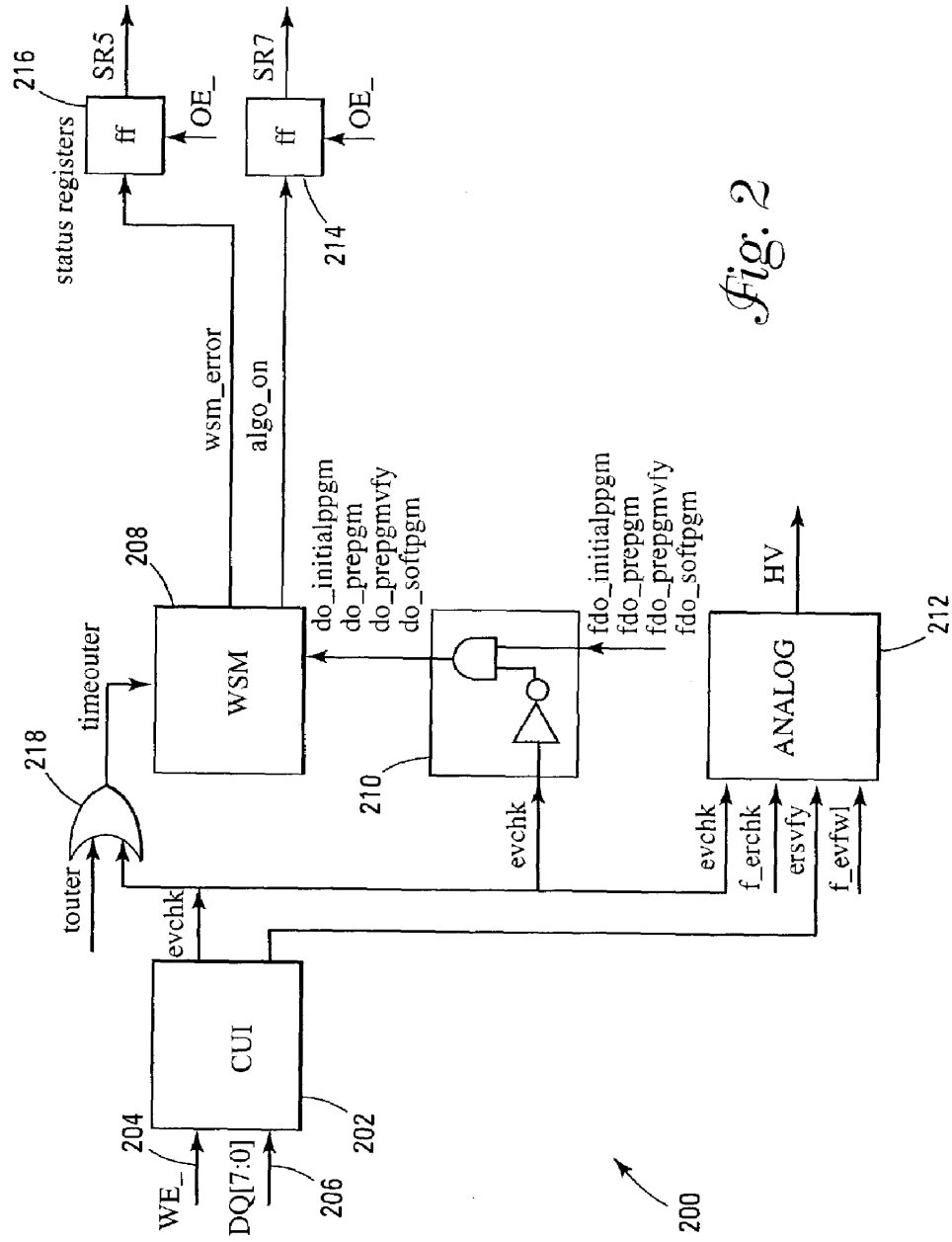
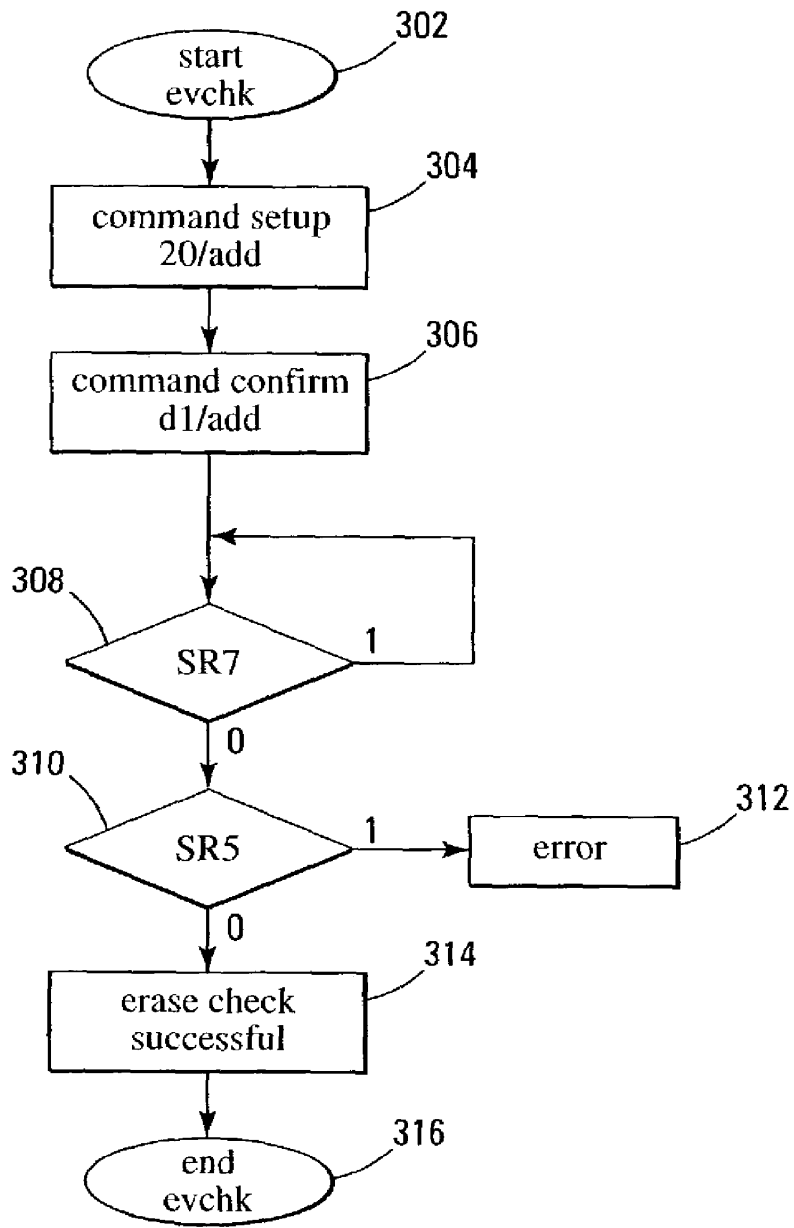


Fig. 2



*Fig. 3*

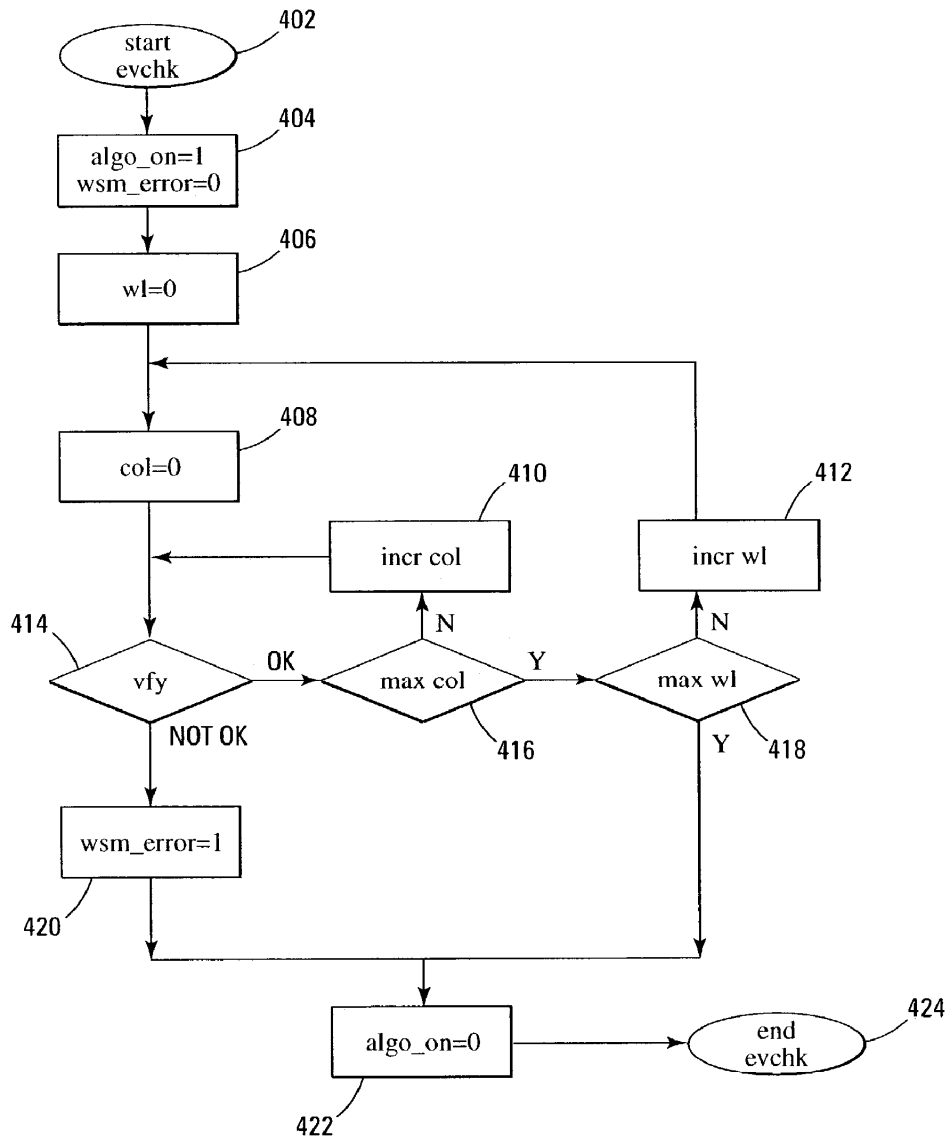


Fig. 4

## BACKGROUND BLOCK ERASE CHECK FOR FLASH MEMORIES

### RELATED APPLICATIONS

This application claims priority to Italian Patent Application Serial No. RM2001A000647, filed Nov. 2, 2001, entitled "Background Block Erase Check for Flash Memories."

### TECHNICAL FIELD

The present invention relates in general to erasing of flash memory devices, and in particular, to an on-chip method and apparatus for performing an erase check of each single block of the flash memory with a known margin against data gain, with minimal time loss.

### BACKGROUND

"Writing" or "erasing" a flash memory cell corresponds to shifting the threshold voltage ( $V_t$ ) of the cell up or down in relation to the reading voltage applied to the gate of the cell. For example, using a read voltage of 5.0 V, the cell is considered erased if its  $V_t$  is 4.0 V or less (with a 1.0 V erase margin). The cell is considered written when its  $V_t$  is shifted to 6.0V or more (with a 1.0 V write margin). The margin is necessary because the cell may slightly change its  $V_t$  when it is cycled with multiple write/erase operations (assuming fixed length and numbers of write/erase pulses), or it may simply change over time during storage. The  $V_t$  increase of an erased cell is dubbed "data gain" while the  $V_t$  decrease of a written cell is dubbed "data loss." Usually chips are erased before being shipped to the customer. A small data gain/data loss is typical for flash memory technology and it can be tolerated. Excessive data gain and data loss may, however, cause errors in reading the flash memory.

Erasing a flash memory with a given margin against data gain requires a complex algorithm. The flash memory chips usually contain internal circuits to erase single blocks of memory cells, then the entire memory, with a specified erase margin. The full internal erase-erase check algorithm involves many steps such as Pre-program, Pre-program Verify, Erase Verify, Erase, Depletion check, Compaction, Erase Verify. The Erase Verify step checks that all cells are erased with a desired margin. If the Erase Verify does not give the expected result, the chip will cycle over some of the above steps. Consequently, the overall erase-erase check operation is quite long. For example, for a 32M flash, it may take up to 20 seconds on flash memory test equipment, which may be up to 40% of the total test time. Even more time is needed for larger memories.

It is possible to erase the memory without making use of the internal algorithm, by using a simplified external erase algorithm with parameters specified by the flash test equipment. This is normally done by flash manufacturers at the time of the product final test. The external algorithm does not perform complex cycles, avoiding increased testing time. In most cases, the external algorithm used at final test is sufficient for a good erase. However, a few cells in some memory chips may be imperfectly erased and thus be more susceptible to data gain. With the external algorithm, it is not guaranteed that all of the chips will be erased with an adequate safety margin. Some chips, particularly those that have been in storage for a long period of time will be subject to data gain. The customer can follow three possible strategies to write data into flash memories on the production line:

- 1) The customer can assume that the flash memory chip is completely erased and proceed to write data into the memory without any prior check. In this case the customer does not spend time to perform erase checks but if the memory is not completely erased there can be errors in the data written or if the memory has no safe erase margins there may be future data corruption due to data gain or disturbance.
- 2) The customer can perform a regular read of the entire block and see if it is erased before writing new data. This regular read is not a background operation, it can only be performed location by location. Furthermore, a regular read can only be performed at a fixed reference value (typically 5V) and no safety data retention margins are guaranteed. The customer spends time for this regular read and still risks future data corruption.
- 3) The customer can perform a regular erase before writing. In this case, the customer can be sure that the block is erased with safe margins but this is a time consuming operation that has a cost. It would thus be desirable to provide a more efficient method of ensuring that flash memory are completely erased to adequate safety margins before they are installed by customers.

### SUMMARY

The above-mentioned problems with traditional erase and erase verify circuits and other problems are addressed by the present invention, at least in part, and will be understood by reading and studying the following specification. The present invention provides an on-chip method to perform the erase check of each single block of flash memory with a known margin against data gain, with virtually no time loss on test equipment. The flash memory customer is only required to send one command to the flash memory, the "Block Erase Check," to initiate the erase check using a safety margin versus data gain that has been pre-selected at the flash memory factory. Once the Block Erase Check command has been made, the chip will proceed in background to perform the erase check. In addition, the Block Erase Check operation is quite fast (0.5 seconds, for example, for a 32M flash memory) and advantageously leaves the microprocessor controlling the testing equipment free for other activities.

The invention further provides apparatus and methods of varying scope.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a memory circuit coupled to a processor and a voltage supply according to an embodiment of the invention.

FIG. 2 is a block diagram of an erase check circuit for a flash memory according to an embodiment of the invention.

FIG. 3 is a flow diagram of an erase check routine according to an embodiment of the invention from the standpoint of a user or external device.

FIG. 4 is a flow diagram of an erase check routine according to an embodiment of the invention from an internal standpoint.

Although, various embodiments have been illustrated using particular electronic components it will be understood by those of ordinary skill in the art that other circuit elements could be implemented and that the present invention is not limited to the arrangement of circuit elements disclosed. Moreover, it will also be understood in the art that the

present invention could be used in connection with non-volatile memory devices other than flash memory. Therefore, the present invention is not limited to an erase check circuit for flash memory.

DETAILED DESCRIPTION

FIG. 1 shows a computer system 100 including a memory circuit 110, a power supply 130 and a processor 140. Memory 110 includes a memory array 112 of nonvolatile memory cells (which can be flash memory cells), a circuit for performing block erase check operations 200, and a controller 120 that controls detailed operations of memory 110 such as the various individual steps necessary for carrying out writing, reading, and erasing operations. Memory 110 also includes an address decoder circuit 122 for decoding and selecting addresses provided by processor 140 to access appropriate memory cells in memory array 112, and an I/O circuit 124 for providing bi-directional communications between processor 140 and memory circuit 110.

As with many flash memory operations, internal (on-chip) write and erase algorithms are started by commands given to the flash memory by the user or an external device such as processor 140. In the present invention processor 140 may be part of a flash memory user system or may be included in flash memory test equipment. A schematic diagram of an on-chip circuit 200 for performing the block erase check operations according to an example of the present invention is shown in FIG. 2. Circuit 200 may include a command user interface or command interface (CUI) 202 that recognizes all flash memory commands including commands specific to the erase check operation of the present invention. CUI 202 may also provide various output signals for operation of components of the flash memory. CUI 202 may be activated by the write enable signal (WE\_) on write enable line 204 and may receive commands on one or more input/output (I/O) lines 206 (shown in FIG. 2 as 8 lines and designated DQ[7:0]). The commands on the I/O lines 206 may be codes such as commands from external testing equipment and may be latched into the memory by the WE\_ signal, for example, when WE\_ is low. The commands are interpreted by CUI 202 logic and executed by a Write State Machine (WSM) 208, which may independently supervise execution of the entire write and erase algorithms.

The present invention includes execution of one or more commands, referred to collectively as a "Block Erase Check." The block erase check enables WSM 208 to internally start and independently execute the erase check or verify operation of all the locations of the selected block (sector) using proper safety margins.

FIG. 3 shows a flow diagram of the operation of a basic block erase check routine evchk (Block Erase Check) from the standpoint of a user or external device, according to the present invention. The Block Erase Check command may be given in two cycles. In command setup block 304, which follows start block 302, a set-up command (code 20) is applied to the I/O lines 206 by an external device, such as the flash test equipment. In addition, the address (add) of the sector or block to be verified is applied to the chip memory address lines (not shown).

The erase check routine starts once the second cycle, shown at block 306, confirmation (command confirm) is given (code d1) on the I/O lines 106 while the address (add) of the sector to be verified is applied to the address lines.

Circuit 200 also may include one or more status indicators readable by external devices, such as status registers 214 and 216. Status register 214 (SR7), shown as a flip-flop, indi-

cates when WSM 208 has completed scanning all the sector locations. When the output of status register 214 is zero WSM 208 has completed address scanning. A second status register 216 (SR5), which may also be a flip-flop, flags whether the Block Erase Check operation has been successfully completed. For example, if status register 216 is zero, it means that the Block Erase Check operation has been successful. Both registers 214 and 216 may be read using the Output Enable OE\_ signal, as shown in FIG. 2.

While there are a number of signals output by CUI 202, to simplify the drawing, only two are illustrated in FIG. 2. The first signal, Evchk, enables the Block Erase Check operation. The second signal, ersvfy, enables the normal Erase Verify operation.

For manufacturing flexibility, flash memories are usually provided with fuses to trim the verify voltages during the testing phase. Analog block 212 is designed to adjust its output voltage HV according to the signals f\_evfwl coming from a set of trimming fuses (not shown in the figure) for the normal Erase Verify step, and according to the signals f\_evfwl coming from another set of trimming fuses (not shown in the figure) for the Block Erase Check operation of the present invention. The HV signal is used to read the memory cells and is applied to the word line of the memory array (not illustrated). The HV trimmable value is typically in the range 3.25V-5V. The normal reading word line voltage is 5V.

The erase margin or erase verify value used in the erase operation executed with the internal algorithm is typically about 3.75V. The Block Erase Check operation need not be performed using this value. If a tolerable data gain is 0.5 V, for example, the Block Erase Check command (20,d1) may be performed using a typical HV voltage of 4.25 V on the memory word lines. This will ensure that only cells in which there has been excessive data gain will fail an erase check.

As noted above, WSM 208 manages all the basic operations involved in an erase or program algorithm. WSM 208 can perform or skip some of these basic operations according to a set of configuration fuses (not illustrated) that are provided for test flexibility.

Signal coming from configuration fuses include:

fdo_initialppgm	to allow the initial pre program operation
fdo_prepgm	to allow pre program operation
fdo_prepgmvfy	to allow pre program verify operation
fdo_softpgm	to allow depletion check/recovery operation

Usually all the above operations are enabled for the internal erase algorithm, but during the Block Erase Check they may all be disabled by the signal evchk through logic block 210, which provides combinational logic to disable fdo\_initialppgm, fdo\_prepgm, fdo\_prepgmvfy, fdo\_softpgm when evchk is active. During Block Erase Check, only Erase and Erase Verify operations need be enabled for WSM 208.

In the standard internal erase algorithm, the signal touter, shown as one input to two input OR gate 218, stops further operation of WSM 208 when a time-out condition has been reached or when the maximum erase pulse count has been reached. This is needed to prevent WSM 208 from locking in a loop in attempting to erase a failed cell. In Block Erase Check, timeout is given by default, since evchk forces touter, the output of OR gate 218 to "1". WSM 208 will only execute one erase check and nothing else, flagging an error immediately if an erase check fails.

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A flow diagram showing the operation of WSM 208 in performing the Block Erase Check from an internal standpoint is shown in FIG. 4. When the Block Erase Check command is recognized, operation begins at 402. At 404 the algo\_on signal is set to "1" and the error flag wsm\_error is initialized to "0." Blocks 406 and 408 show initializing of word line counter (wl) and column counter (col) (inside WSM 208) to "0." The memory location at address (wl, col) is erase verified at 414. If the result of the check operation is OK, the column and word line counters are incremented (incr col and incr wl) at 410 and 412, respectively. Assuming no errors, incrementing continues until the maximum (max col and max wl) values are reached at 416 and 418. Then, at 422 the algo\_on signal is set to "0" to flag that the operation is completed. The first time an erase check operation fails, the signal wsm\_error is set to "1" at 420 and the algorithm is immediately stopped, setting algo\_on to "0" at 422. The operation concludes at end evchk, block 424.

## CONCLUSION

A flash memory erase check circuit is disclosed. One embodiment includes an on-chip circuit that checks that the flash memory chip has been and continues to be thoroughly erased, even after data gain may have resulted, for example, from a long period of storage. The circuit may carry out the erase check operation in response to a single off-chip command. Another embodiment includes a method for performing the on-chip erase check. Embodiments of the present invention are fast, because unnecessary interactions between controller and memory are avoided. The present invention further provides safe erase checking, because the voltage used in the Erase Block Check insures an adequate margin versus further data gain. In another aspect the present invention may advantageously work in the background, because it is internally executed by a state machine upon receiving an external command from test equipment.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement, which is calculated to achieve the same purpose, may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. A method for performing an erase check of a previously erased non-volatile memory, comprising:

initiating a block erase check of the non-volatile memory on an on-chip state machine in response to at least one off-chip signal;

executing the block erase check on the on-chip state machine to a predetermined margin; and

providing a signal readable off-chip if an error is detected; wherein the predetermined margin is closer to a read voltage value than a normal erase verify margin for the non-volatile memory.

2. The method of claim 1, wherein the block erase check may be initiated in response to a single off chip command.

3. The method of claim 1, wherein the state machine terminates the block erase check immediately upon detecting an error.

4. The method of claim 1, wherein the at least one off-chip signal is interpreted by a command interface.

5. The method of claim 1, wherein the predetermined margin is set by one or more on-chip fuses.

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6. The method of claim 1 further comprising temporarily disabling normal on-chip erase operations.

7. The method of claim 1, wherein the non-volatile memory comprises a flash memory.

8. The method of claim 1, wherein the signal readable off-chip if an error is detected is stored in a register.

9. A block erase check apparatus integrated with a non-volatile memory device on a semiconductor chip, comprising:

an input-output device that communicates with an off-chip device;

a command interface that interprets signals received by the input-output device;

a state machine that executes a sequence of erase check operations in response to one or more signals from the command interface, wherein the state machine executes the erase check operations according to a predetermined erase check margin that is different than a predetermined erase verify margin; and

a register, readable by the off-chip device, that provides status information on the erase check operations executed by the state machine.

10. The on-chip flash memory erase check apparatus of claim 9, wherein the predetermined erase check margin represents a greater tolerance than a normal erase verify margin.

11. The on-chip flash memory erase check apparatus of claim 9, wherein the on-chip flash memory erase check operation is performed by the state machine in response to a single command from the off-chip device.

12. A method for performing an erase check of a flash memory, comprising:

sending a command to an on-chip state machine for initiating a block erase check operation;

executing the block erase check operation on the on-chip state machine with reference to a predetermined voltage, wherein the predetermined voltage is different than a normal erase verify voltage; and

signaling if an error is encountered while performing the block erase check operation.

13. The method for performing an erase check of a flash memory of claim 12, wherein the predetermined voltage is fixed by setting one or more on-chip fuses.

14. A system comprising:

a non-volatile memory coupled to a processor and a power supply, and a memory erase check circuit integrated on-chip with the non-volatile memory, comprising:

an input-output device for communicating with an off-chip device;

a command interface that interprets signals received from the input-output device;

a state machine that executes a sequence of erase check operations in response to one or more signals from the command interface, wherein the state machine executes the sequence of erase check operations according to a predetermined erase check margin that is different than a normal erase verify margin; and

a signaling device, readable by the off-chip device, that provides status information on the erase check operations executed by the state machine.

15. The system of claim 14, wherein the state machine executes the sequence of block erase check operations in the background.



16. The system of claim 14, wherein the predetermined erase check margin represents a greater tolerance than the normal erase verify margin.

17. The system of claim 14, wherein the on-chip flash memory erase check operation is performed by the state machine in response to a single command from the off-chip device.

18. The system of claim 14, wherein the sequence of block erase check operations ends upon encountering a cell that has not been erased to the predetermined erase check margin.

19. A method for checking that non-volatile memory has been erased, comprising:

performing a normal erase operation, including an erase verify, of the non-volatile memory to a first predetermined margin;

performing a block erase check of the non-volatile memory to a second predetermined margin subsequent to the normal erase operation, wherein the second predetermined margin is different than the first predetermined margin; and

providing a signal readable by an off-chip device if an error is detected.

20. The method of claim 19, wherein the block erase check may be performed in response to a single off chip command.

21. The method of claim 19, wherein the block erase check is controlled by an on-chip state machine.

22. The method of claim 19, wherein the erase check operation is terminated if an error is detected.

23. The method of claim 19, wherein each predetermined margin is set by one or more on-chip fuses.

24. The method of claim 19, wherein the second predetermined margin is greater than the first predetermined margin.

25. The method of claim 19, wherein initiating the on-chip block erase check operation comprises temporary disabling of normal on-chip erase operations.

26. The method of claim 19, wherein the non-volatile memory comprises a flash memory.

27. A system comprising:

a non-volatile memory chip coupled to a processor and a power supply, and

a memory erase check circuit integrated on-chip with the non-volatile memory, comprising:

an input-output device for communicating with an off-chip device;

a command interface that interprets signals received from the input-output device;

control circuitry that executes a sequence of erase check operations subsequent to normal erase and erase verify operations and in response to one or more signals from the command interface, wherein

the control circuitry is adapted to perform the erase check operations at a different margin than the erase verify operations; and

a signaling device, readable by the off-chip device, that provides status information on the erase check operations executed by the state machine.

28. The system of claim 27, wherein the control circuitry executes the sequence of erase check operations in the background.

29. The system of claim 27, wherein the control circuitry executes the sequence of erase check operations according to a predetermined erase check margin.

30. The system of claim 29, wherein the predetermined erase check margin represents a greater tolerance than a normal erase verify margin.

31. The system of claim 27, wherein the sequence of erase check operations is performed by the control circuitry in response to a single command from the off-chip device.

32. A block erase check apparatus integrated with a non-volatile memory device on a semiconductor chip, comprising:

an input-output device that communicates with an off-chip device;

a command interface that interprets signals received by the input-output device;

a state machine that executes a sequence of erase check operations subsequent to a normal erase and erase verify, and in response to one or more signals from the command interface, wherein the state machine is adapted to perform the erase check operations at a different margin than the erase verify; and

a register, readable by the off-chip device, that provides status information on the erase check operations executed by the state machine.

33. The on-chip flash memory erase check apparatus of claim 32, wherein the state machine executes the sequence of erase check operations according to a predetermined erase check margin.

34. The on-chip flash memory erase check apparatus of claim 33, wherein the predetermined erase check margin represents a greater tolerance than a normal erase verify margin.

35. The on-chip flash memory erase check apparatus of claim 32, wherein the sequence of on-chip flash memory erase check operations is terminated by the state machine upon detecting a memory cell that fails the erase check.

36. The on-chip flash memory erase check apparatus of claim 32, wherein the sequence of on-chip flash memory erase check operations is performed by the state machine in response to a single command from the off-chip device.