1Tb density, 4 bits-per-cell 3D NAND flash in 110s technology

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Abstract: **1 Terabit density, 4 bits-per-cell 3D NAND flash in 110s technology is presented in this paper. It is possible to operate the memory not only in 4 bits per cell but also on-the-fly single bit per cell to increase distributions separation. Program operation is based on an 8-16 Program algorithm. It is a high-speed device capable of 667 MT/s throughput in ONFI4.0 mode. It is organized in four planes for a multiplane operation with 16kB page size. Periphery is a CMOS under array for high area saving. 4 bits per cell capability was reached using negative voltages for expanded window in the negative region. Array is organized in 74 tiers divided in two superimposed regions. An increased number of WL groups for Read and Program was devised to improve uniformity across tier. Flexible page mapping allows programmable page configuration for optimal management of edge wordlines. The device was designed to achieve tPROG = 3ms, tR = 127µs, ICC quad plane = 39mA, and ICC single plane = 20mA with VPP enabled. Techniques were devised to address first page Read issue, E0 degradation due to hot electrons, and plane-to-plane variations. Typical 1.5V Read window budget (RWB = sum of the Vt separation between adjacent distributions) was demonstrated.**

Index Terms: **3D NAND, flash memories, nonvolatile memory, QLC**

I. Introduction

3D NAND flash technology has significantly improved its performance and reliability, enabling the design of a high-density, 4 bits-per-cell (QLC) device.

This paper describes the first monolithic 1Tb, 4-bits-per-cell device on the market named N18A. The paper is organized in eleven sections. After the introduction, device features and array architecture are described in Section II. Device architecture and zero periphery are described in Section III. Window required for QLC is reported in Section IV. Negative voltage and cell optimization are described in Sections V and VI, respectively. 8-16 Program sequence and QLC Read are reported in Sections VII and VIII, respectively. Design techniques to manage RWB (WL grouping, auto Read calibration, Read reset, Vreg per plane and tile groups (TG) scrambling, and asymmetrical seed) are described in Section IX. Short notes about competition are reported in Section X, and the conclusion on N18A QLC capability is reported in Section XI.

II. N18A Features and Array Architecture

In this section, N18A array architecture is described. N18A is 1Tb memory organized in four planes. This device was designed to be either 4 bits per cell (QLC) or 1 bit per cell (SLC) on the fly. Table I reports the main specification and features. N18A is 3D NAND with 74 stacked wordlines and 12 SGD (sub blocks) with four segmented SGS. Array block architecture is reported in Fig. 1.

Table I
N18A Main Specifications and Features

Feature/Spec	N18A
Density	1Tb (QLC)
Die size	159.68mm^2
Cell structure	74-tiers 3D 12 SGD ShiftP
Multi-plane CMD	4 x 16KB
# of pages/block	3072
# of blocks/plane	684 + 16 + 34 + 2
ECC	ECC for RBER of 1E-2
External VPP	10.8–13.2V/12.0–14.6V
tPROG eff	3ms
tR avg	127µs
SLC tR	52µs

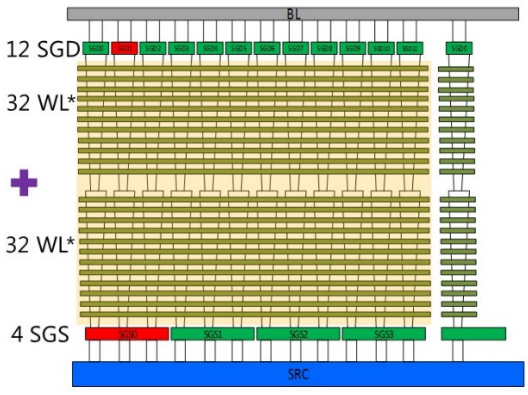

Fig. 1. Block architecture.

III. Device Architecture and Zero Periphery

CMOS-under-array (CuA) has been proposed in [1]. It is an important technology innovation for the Micron 3D NAND, and since the beginning of the 3D NAND CuA,

has been proposed for pitch cell (X/Y circuitry). Zero periphery architecture is the evolution of CuA where the entire periphery is moved under array allowing considerable area saving (~10–20% depending on the specific die size) compared to previous architectures [2].

In Fig. 2, the N18A device architecture is reported. Micron's 3D NAND string driver has been designed to stay under the array as well as the page buffer (PB), thus allowing a compact layout and loading optimization. Zero periphery technique allows to move the full periphery, except the pads, into the core area. Large-area pockets are in fact created abutting two tile groups along the WL direction and abutting two tile groups along the BL direction, thus allowing allocation in the core area an entire subsystem like logic, charge pumps, global drivers, and so on.

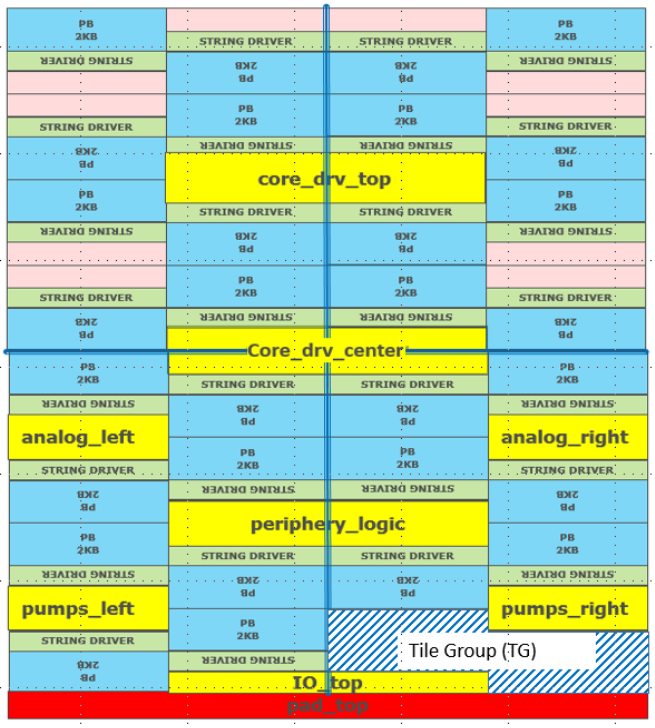

Fig. 2. N18A device architecture.

IV. QLC Window

QLC has 4 bits/cell in 16 possible VT states (L0 to L15). It is thus necessary to allocate 14 VT states within the total available window. The typical TLC window is no longer enough to guarantee sufficient distance between adjacent QLC states. A QLC window expansion of about 20% was obtained using negative VT cell allocation, as reported in Fig. 3.

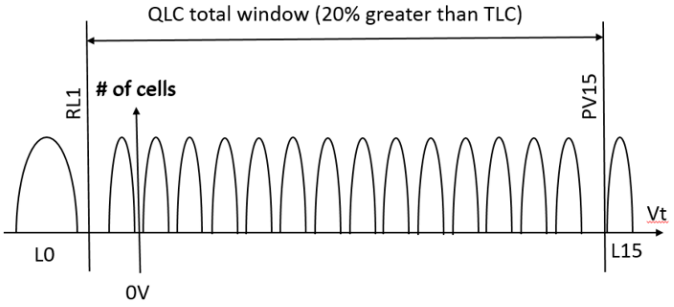

Fig. 3. QLC total available window.

It was necessary to take two actions for the capability of VT allocations below 0V: the first action was taken by design team introducing a charge pump generating negative voltage and designing all the switching circuits to allow its propagation into the array, and the second action was taken by the process integration team performing cell modification and allowing deeper Erase VT saturation.

V. Negative Voltage

Delivery of a negative voltage to the array is achieved using a negative charge pump and vwlrv (voltage for WL Read and Verify) driver. As reported in Fig. 4, the negative pump can reach approximately –3V when it is not loaded and approximately 11mA when it is fully loaded. A negative charge pump generates the negative voltage vneg that can be trimmed from –0.125V to –3.071V using fuses.

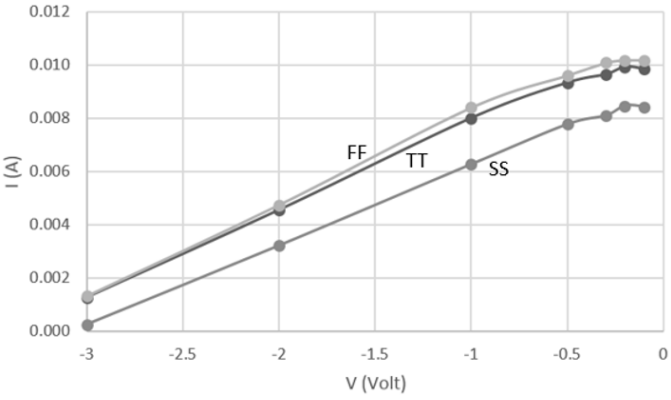

Fig. 4. Negative charge pump IV.

The block schematics of the vwlrv driver is reported in Fig. 5. It is composed by an amplifier generating the vwlrv output. The driver contains a switch controlled by pos_sw signal. If pos_sw = 1, vwlrv can cover only a positive range, depending upon the value of vref (set by a DAC), as described in (1). If pos_sw = 0, vwlrv can cover both negative and positive ranges depending upon vref and vpos_ref (set by a DAC), as described in (2).

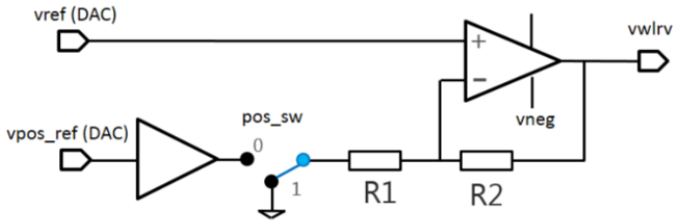

Fig. 5. A vwlrv driver.

$$If\ pos\_sw = 1, then\ vwlrv = vref * \left(1 + \frac{R2}{R1}\right) \quad (1)$$

$$If\ pos\_sw = 0, then\ vwlrv = vref * \left(1 + \frac{R2}{R1}\right) - vpos\_ref * \frac{R2}{R1} \quad (2)$$

Table II presents vwlrv value ranges, if the vneg pump was trimmed to –2.865V.

Table II
vwlrv Ranges

DAC (hex)	pos_sw = 0	pos_sw = 1
000	–2.865	+0.010
...	...	...
0FF	–0.135	+2.560
11F	+0.185	+2.880
...	...	...
3FF	+7.545	+10.240

VI. QLC Capability: Cell Optimization

It is not enough to provide negative voltage to increase the total available window. It is also necessary to have a NAND cell that can reach VTs well below zero at time0 and after Program/Erase (PE) cycles. A previous NAND cell, engineered for TLC and called CR8, was not adequate for QLC because its deepest negative VT saturated at levels that were not deep enough. The CR8 cell was then modified to obtain a new cell, called CR9, that had deeper negative VT saturation [3]. The structures of the CR8 and CR9 cells are reported in Fig. 6, showing the trapezoidal shape of CR9 [3].

In CR9 erased Vt saturation occurs at a lower voltage –6V instead of –4.3V, as reported at time0 and for typical inner WL in Fig. 7, thus allowing a bigger window.

The trapezoidal shape of CR9 is just a part of the cell optimization. Further improvements must be considered to address the trap-up issue and floating gate-to-floating gate interference (FGFG), as reported in detail in [3] and [4]. Trap-up is defined as the Vt degradation due to trapped charges. The optimized CR9 allowed doubling of the trap-up performances at time0 and at 3000 cycles, resulting in more uniform trap-up performances along the pillar [3]. Optimized control allowed a reduction of 1.5% [3] the FGFG at time0 and with cycling.

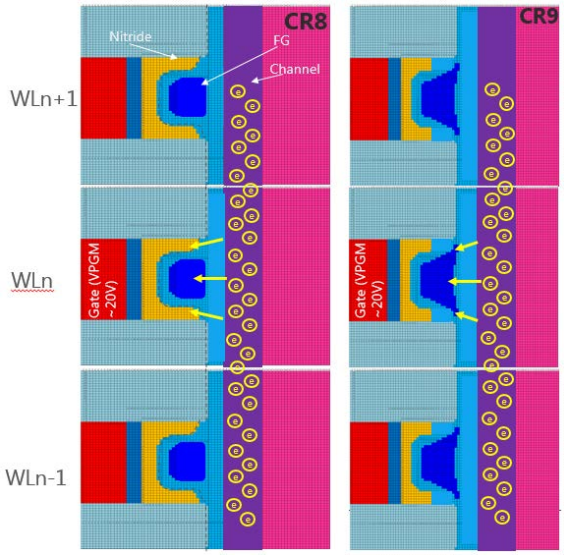

Fig. 6. Structure of CR8 and CR9 cells.

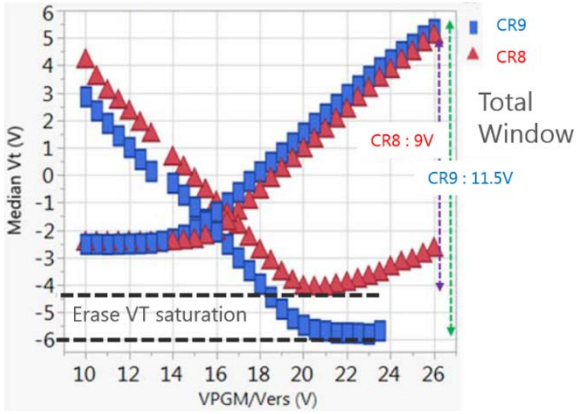

Fig. 7. CR8 and CR9 erased VT saturation.

VII. 8-16 Program Sequence

Each QLC distribution is described by four bits. Each bit is a single element of a set called page: the less significant is called lower page (LP), then we have upper page (UP), then extra page (XP), and the most significant, top page (TP).

In QLC two–pass, 8-16 programming, LP, UP, and XP are programmed during the first programming pass (Fig. 8). The die supports the Read of the LP, UP, and XP data programmed during the first programming pass. The second programming pass requires the availability of LP, UP, XP, and TP, and this can be accomplished in two ways per a fuse: either the host provides the four pages or it provides XP and TP while LP and UP are read internally (pre-Read), assuming the floating gate-to-floating gate interference is low enough to allow clean pre-Read. Choosing proper values for start, step, pass, and inhibit Program voltages, the 8-16 Program algo could achieve typical distribution width adequate for targeted RWB even considering the best and worst sub block differences of approximately 40%, as reported in Fig. 9.

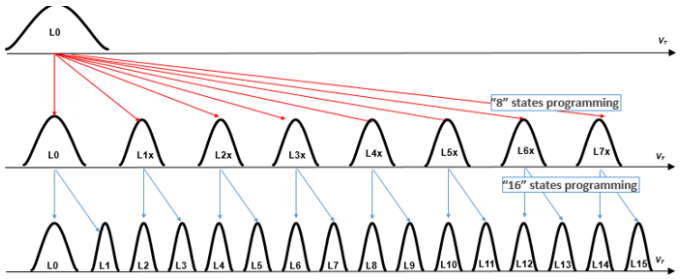

Fig. 8. Two-phase, 8-16 Program technique.

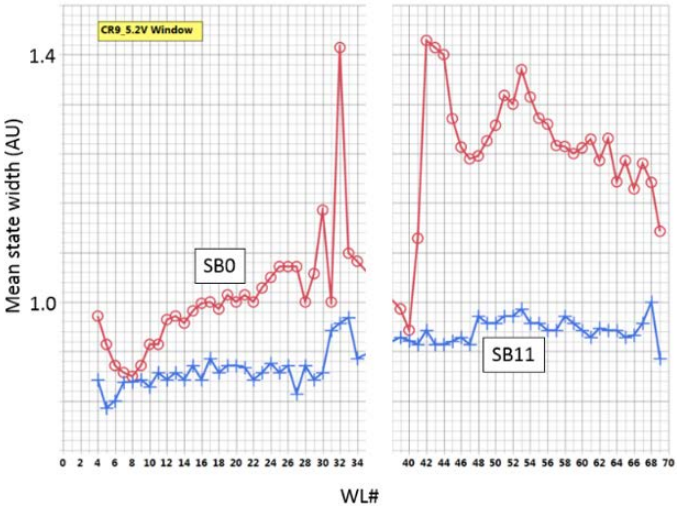

Fig. 9. Typical min state width achievable with 8-16 Program algo [5].

VIII. QLC Read

QLC Read levels and sequences are reported in Figs. 10 and 11, respectively. Due to extension of the window in the negative VT region, some of the Read levels (RL1 and RL2) could be negative.

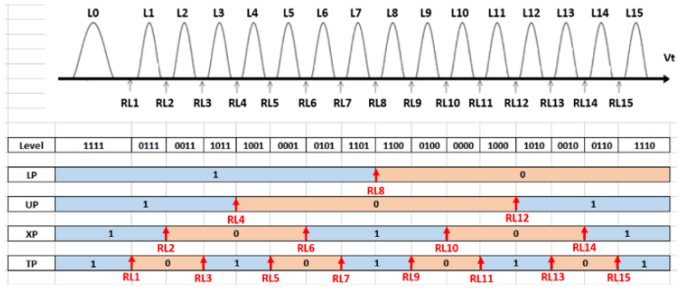

Fig. 10. Read levels for QLC.

IX. Design Techniques to Manage RWB

Achieving safe values of RWB is particularly critical for QLC because there are 16 distributions to be allocated in a Vt window that is not much greater than the Vt window of a TLC device. There are some factors affecting the RWB that need to be considered when placing distributions: nonuniform behavior of electrical characteristics of NAND cells along the string, retention, endurance, first-page Read (FPR) VT instability, and block-to-block VT variability. In addition to some of the cell process optimizations already described, there are proper design techniques to address these issues.

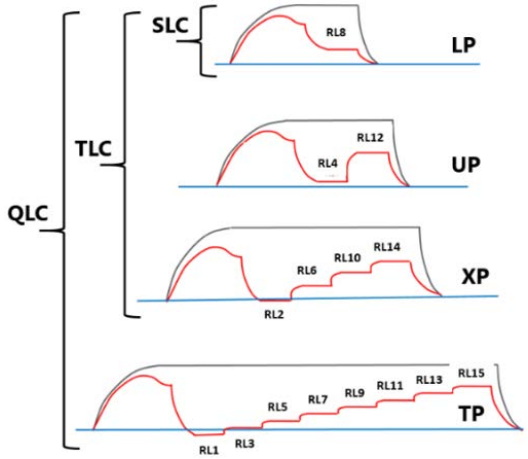

Fig. 11. Read sequence for QLC.

A. Nonuniform Behavior along the String

NAND cell electrical characteristics depend on the position in the string, and for this purpose the string has been divided in groups of WLs that have different values of fuses. In N18A, there are 14 groups for QLC wordlines and 8 groups for edge wordlines, giving the possibility to specify different values such as Read levels, Program Verify levels, and temperature compensation for each group in Read and Verify operations and different values such as start Program voltage, step Program voltage, and Vpass for each group.

B. Retention and Endurance

Retention and endurance are two of the key factors affecting the RWB. Distributions moving down as time progresses and distributions of different placement due to cycling become more critical when passing from the TLC device to QLC device. There are two design techniques to manage the placement shift due to retention and endurance: Read retry (RR) and automatic Read calibration (ARC). These two techniques are deeply described in the N18A design data sheet [6] and have been widely used in past NAND devices. Read retry is a Read technique that is applied by the user when the memory is starting to fail, and frequent error correction code (ECC) is needed to recover errors. At this point, it is possible to perform Read operations using a different set of Read levels per the aging and cycling model devised for the device. Automatic Read calibration consists of performing a measure of the midpoint between a couple of adjacent distributions (valley check) to find the best actual separation point between two adjacent distributions. These best actual separation points are used as new optimized Read levels. It is not realistic to use ARC at every page Read because it is very time consuming. It is possible anyway to perform ARC just once, when it is needed, and store the calibrated values for future Reads. The effect of

ARC is greater for top page at hot temperatures, and it can reduce the raw bit error rate (RBER) by one order of magnitude [7].

C. First Read VT Instability

3D NAND cell Vt can be found in two different states: transient Vt (low Vt) and stable Vt (high Vt), per the fact that the cell underwent a recent stress or the cell had enough time to recover the stress. A detailed description of this mechanism is reported in [8]. The delay needed to pass from transient to stable is variable from cell to cell and is in the range of milliseconds to seconds. The delta Vt between the transient and stable states is in the range of 200mV and varies among cells; therefore, Vt distributions can shift and widen. After a Read is performed in a stable state (first Read), the Vt of the cell shifts to transient state due to Vpass Read stress, and all subsequent Reads performed in a short time will be performed with Vt in a transient state. RWB evaluations showed that the best situation is to have Verify and Read both in a transient state with positive RWB at time0 and after 2K cycles [8].

A design technique called "reset Read" has been devised to clean up the channel and move the cell always in the desired transient state. The reset Read sequence takes between 35µs and is performed by user command soon before each regular Read operation, which is thus performed always in a transient state preventing Vt variability. The reset Read applies to the entire block where the target page belongs. It is performed by ramping all WLs to VpassR (approximately 5.5V). SGS is enabled and source grounded to prevent pillar from boosting. WL recovery drives pillar potential negative. Reset Read demonstrated 50% failing bits recover capability.

D. Block-to-Block Variation

It has been observed that there is a distribution shift along the pillar (known either as intra-block variation or page-to-page variation), among different planes (known either as intra-plane variation or block-to-block variation), or among different die (known as intra-die variation or extended block-to-block variation). This shift is not impacting the distribution separation of a single Read but it reduces the resulting separation of Reads in different places where the Read level is unique. Both page-to-page variation and block-to-block variation can erode the total amount of RWB. Page-to-page variation is mitigated using a proper WL fuse grouping management. To mitigate the page-to-page variation, it is also possible to think about the possibility to use the ARC technique at each Rea, but this impacts Read performance ranging from 25% to 90%, depending on different ARC usage. The block-to-block variation was addressed by a design using two concurrent techniques: tile group scrambling and separated Vreg1 by plane using trimmed by-plane values.

The tile group (TG) scrambling is reported in Fig. 12, and it is aimed to have uniform path to source (SRC) driver independent from the block address. The Vreg1 driver is the driver used for shifting the Read level. Only a single Vreg1 driver is traditionally used for the entire die. In N18A, the Vreg1 driver was replicated for each plane with the possibility of trimming each of them separately. In this way, different source bias values could be achieved for each plane, and sensing offset can be adjusted by plane.

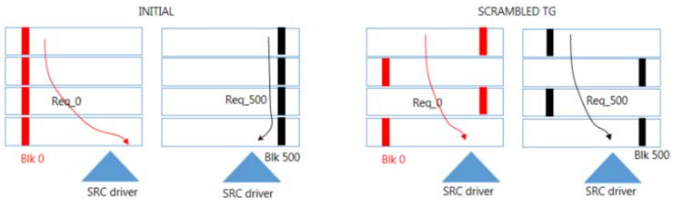

Fig. 12. TG scrambling.

E. Hot Electrons

A critical issue to enable QLC 3D NAND is the control of Vt distribution width. When using a boosting scheme with uniform Vpass on all WLs, no hot electron (hot-e) injection is usually observed in planar NAND because the non-uniformity of the boosting potential is typically small in a monocrystalline-silicon channel. In 3D NAND the mono-crystalline-silicon channel is replaced by a floating body poly silicon pillar, and the lower conductivity of the channel can cause a large voltage drop in the middle of the boosted pillar. This causes hot electron injection in the inner WLs, far from the selectors. Hot electrons can result in severe state width degradation, which is detrimental for QLC applications [9]. A good way to reduce the hot-e disturb is to use asymmetrical seed, performing it with drain side WLs at a positive voltage and/or the source side WLs at a negative voltage rather than all WLs grounded.

X. Competition

On June 2017, Toshiba announced design and production of a 3D NAND Flash memory based on QLC. Samples began shipping early in June 2017 to SSD and SSD controller vendors for evaluation and development purposes. Target applications will be enterprise and consumer SSD, tablets, and memory cards. Toshiba showcased this device at the Flash Memory Summit 2017. Features of N18A and Toshiba devices are reported in Table III.

Table III
N18A versus Toshiba

Feature	Toshiba	N18A Micron
Technology	BiCS	VNAND
Tiers	72	74
Density per die (Gb)	768	1000
Density per 16-stack die (TB)	1.5	3

XI. Conclusion

N18A targeted customers are low-cost SSDs for hard-disk replacement, low fill per day SSDs, and very high-capacity SSDs for datacenters. N18A showed QLC capability per customer needs. Typical QLC single page distributions are reported in Fig. 13.

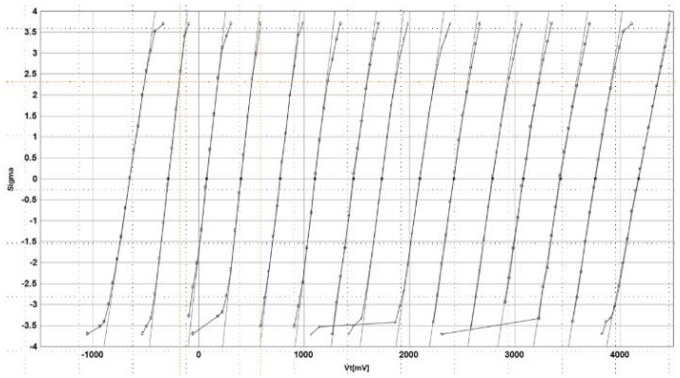

Fig. 13. Typical N18A QLC distributions.

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In 2004, he joined Micron Semiconductor Italia (Avezzano, Italy) and currently is a Principal Design Engineer.

Mr. Moschiano holds 82 U.S patents and 96 U.S patent applications. He has also co-authored five technical articles. He is Distinguished Member Technical Staff at Micron.

L. Pilolli received a master's degree in electronic engineering from the University of L'Aquila (Italy) in 2005.

In 2006, he joined Micron Semiconductor Italia (Avezzano, Italy) where he currently works as a Principal Design Engineer. His research interests span from analog and digital design to high-speed IO interfaces and protocols.

Mr. Pilolli holds eight international patents, seven U.S. patents, and 11 U.S. patent applications. He has co-authored three technical articles.

M. Rossini received a master's degree in electronic engineering from the University of Rome "La Sapienza" (Italy) in 1987.

From 1985 to 1988, he worked at CMT Informatica as a Firmware Engineer, and in 1988, he joined Texas Instruments (Rieti, Italy). In 1998 he transitioned to Micron Semiconductor Italia (Avezzano, Italy) and currently works as a Senior Design Manager.

Mr. Rossini holds six U.S. patents and three U.S. patent applications. He has co-authored four technical articles.

G. Santin started his career in 1978 with Texas Instruments and progressed through several assignments in the field of integrated circuits design, both in Italy and abroad in Japan and the United States. In 1998, the Texas Instruments memory division was acquired and became Micron Semiconductor Italia (Avezzano, Italy). Since then, he has the responsibility of the development of the memory core design and architecture of all flash memories designed in Italy.

Mr. Santin holds 105 patents, all in the field of nonvolatile memories, and has 87 patents pending. He is a regular lecturer at the University of L'Aquila covering topics about NAND flash design to postgraduate students of the Electronics Engineering school. He is Distinguished Member Technical Staff at Micron.

U. Siciliani received a master's degree in electronic engineering from the University of Rome "La Sapienza" (Italy) in 2000.

In 2001, he joined STMicroelectronics (Catania, Italy, and later Palermo, Italy). In 2005, he joined Infineon (Padova, Italy), and, in 2006 he transitioned to Qimonda (Padova, Italy). In 2008, he joined Micron Semiconductor Italia (Padova, Italy) and currently works as a Senior Design Manager.

Mr. Siciliani holds two U.S patents and seven U.S patent applications. He has co-authored three technical articles.

S. Spagliccia received a high school diploma in electronics from L'Allievi Technical Institute (Terni, Italy) in 1975.

He joined Texas Instruments (Rieti, Italy) in 1977. After the acquisition of the memory business unit by Micron Technology, Inc. in 1998, he joined Infineon (Padova, Italy) in 2004 and Qimonda in 2006 and supported their memory products business. In 2008 he joined Micron Semiconductor Italia (Padova, Italy) where he currently works as a Layout Manager.

B. Tronca started his career developing very high-density PCBs in AS&T Srl (Italy). In 1993, he was hired by Texas Instruments (Rieti, Italy) as an IC Layout Engineer in Memory R&D. He joined Micron Semiconductor Italia (Avezzano, Italy) in 1999 and currently works as a Senior Layout Manager.

A. G. Xotta received M.S. and Ph.D. degrees in electronic engineering from the University of Padova (Italy) in 1999 and 2003, respectively. He held a postdoctoral position in the Department of Information Engineering at the University of Padova from 2003 to 2005.

He joined Infineon Technologies and Qimonda Italy (Padova, Italy) in 2005 and 2006, respectively. He joined Micron Semiconductor Italia (Padova, Italy) in 2008 and now is a Principal Design Engineer.

Dr. Xotta has authored 11 international IEEE publications.

A. Mohammadzadeh received an M.S. degree in computer architecture/ engineering from the University of Tehran (Iran).

He worked at Azalea Microelectronics for two and a half years. During that period, he was part of a small design team working on the design and test of embedded NOR flash chips. In 2005, he joined Micron Technology, Inc. (Milpitas, California USA) and has since held various roles from Design Engineer to Senior Logic Design Manager in the Design Engineering department of Nonvolatile Memory group.

Mr. Zadeh holds five U.S. patents with four patents pending.

Q. Tang received B.S. degrees material science and engineering and in electronic engineering and computer science and an M.S. degree in material science and engineering from Tsinghua University (Beijing, China) in 1996 and 1998, respectively. He received an M.S. degree in electrical engineering and a Ph.D. degree in material science and engineering from Stanford University (Stanford, California USA) in 2000 and 2003, respectively.

He worked in Micron Flash Design team from 2003 to 2007. He rejoined Micron Technology, Inc. (Milpitas, California USA) in 2012 after working on Read channel SOC and SerDes for more than five years at Marvell (Santa Clara, California USA).

T. Vali received a degree in electronic engineering from Roma University "La Sapienza" (Italy) in 1987.

He joined Texas Instruments Italy as a Product Engineer in 1989 and currently works at Micron Semiconductor Italia (Avezzano, Italy) as the Senior NVE EMEA Director.

Mr. Vali holds 75 U.S. patents and is co-author of eight articles in the field of nonvolatile memory.

R. Ghodsi earned a bachelor of engineering degree *(with honors)* and a Ph.D. degree in electrical engineering from the University of Queensland (Brisbane, Australia).

He is Vice President for Design Engineering and Nonvolatile Memory at Micron Technology, Inc. (Milpitas, California USA). He is responsible for the worldwide operation of the nonvolatile design organization, including design centers in California, Japan, Italy, and China. He joined Micron in 1999 and has held various senior engineering and management positions in flash memory and NAND product development. He was appointed to his current position in 2013.

Throughout his more than 20-year career, Dr. Ghodsi has made significant technical contributions in the areas of product design, device technology, and design architecture innovations through patents and refereed technical conferences presentations and journal publications.