

LTE Simulator Relies on Xilinx Virtex-5 FPGAs

Powerful programmable logic platform enables Prisma Engineering to provide reconfigurable radio test equipment for all cellular networks.

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LTE (Long Term Evolution), the new 3GPP standard for broadband mobility, disrupts the existing paradigms of cellular networks. In addition to high-spectral-efficiency radio techniques, LTE boasts a very simplified architecture in comparison to the prior-generation UMTS and GSM standards. Evolved Node-B's, the radio-access part of the LTE system, are the edge between the radio and all-Internet Protocol core networks. This architecture makes it impossible to monitor and test the equivalent of intermediate links in UMTS. An effective testing of LTE network elements must involve the radio interface.

This is exactly the challenge addressed by our design team in Prisma Engineering's Line Server Unit (LSU) UeSIM LTE. The simulator is a complete solution for all LTE testing needs, allowing network equipment designers to stress and monitor both the air interface and the core network. This single hardware platform can simulate up to 1,024 pieces of user equipment per sector. Load-and-stress and functional testing over the radio interface encompass complete LTE protocol stacks and their applications. A radio front end handles bandwidths of 5, 10, 15 and 20 MHz in a native multiple-input, multiple-output (MIMO) design.

Three Xilinx® Virtex®-5 FPGAs (XC5VSX50T) reside at the heart of this advanced simulator, enabling a high level of software-defined radio reconfiguration. Our team at Prisma Engineering, which is headquartered in Milan, Italy, quickly realized we needed a powerful and reprogrammable architecture in order to gain the flexibility to address all these radio access standards using the same board. Our main goal was, as our CEO, Enrico Bendinelli, put it, “to create the industry’s most flexible and easy-to-use management software.”

Two user test tools—the LTE Test Manager (primarily for LTE equipment vendors) and the Quick GUI (primarily for LTE network operators)—are available. The Quick GUI provides pass/fail-type testing scenarios while the Test Manager allows for more complex analysis.

LSU UeSIM LTE Architecture

The LSU UeSIM simulator is based on a CompactPCI standard architecture comprising a protocol-processing unit (PPU) board, a software-defined radio (SDR) board and two radio modules for MIMO operations.

Based on Intel technology, the PPU board, which is the main processor card, is able to manage multiple SDR boards in order to improve the load-and-stress capacity. The software-defined radio board is designed to extend the operation of our previous LSU systems on the radio interfaces. The CompactPCI radio mezzanine cards provide radio-frequency (RF) transmission/reception capability at different radio standard bandwidths: GSM (850 and 900 MHz; 1.8 and 1.9 GHz), LTE (700 MHz, 2.1, 2.3, 2.5 and 2.6 GHz) and WiMAX (2.4, 3.5 and 5 GHz).

SDR Card Architecture

The SDR card is a high-performance platform integrated within the LSU hardware/software environment to extend the connectivity of the system with the baseband (CPRI/OBSAI), the radio interface or both. The card supports different wireless standards such as GSM/EDGE, UMTS, HSPA, WiMAX and LTE using different external radio modules operating in the specific frequency bands.

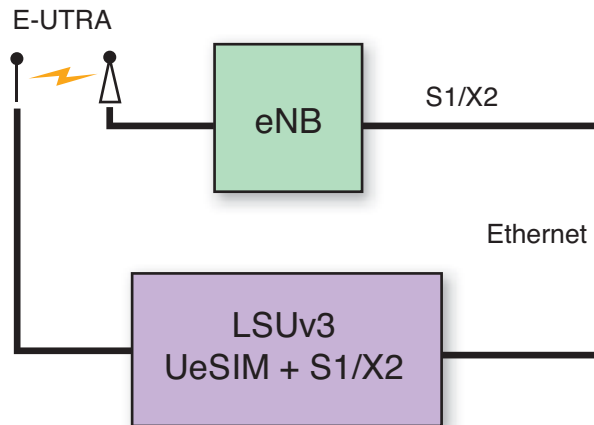


Figure 1 – In an LTE test scenario, the simulator either replaces a radio sector or provides a test interface for the core network.

We completed the design of the Xilinx-based SDR card with three 1-GHz Texas Instruments DSPs (we chose the TMS320C6455 device) and two pairs of Analog Devices analog-to-digital (AD9640) and digital-to-analog (AD9779) converters. The clocking network, based on an Analog Devices AD9549, provides a very high, flexible timing base for the conversion and digital signal-processing devices (FPGAs, DSPs).

LTE Elaboration Datapath

Prisma divided the LTE elaboration datapath into two sections: the radio front end, which we implemented in an FPGA, and the physical-resource allocation and data- and control-channel termination, which we implemented in a DSP.

In the uplink direction, one DSP handles MAC-layer to physical-layer exchange and some functions of the physical layer. It



Figure 2 – Xilinx Virtex-5 FPGAs reside on the LSU’s software-defined radio card, along with TI DSPs.

provides coding, interleaving, scrambling, symbol mapping and subcarrier allocation with reference signal (pilots), source data and control channels. Discrete Fourier transform (DFT) functions transform data from different terminals according to the SC-FDMA standard. The system transfers every OFDM symbol to the uplink FPGA using an EMIF interface.

This FPGA changes the data rate from 125 MHz (DSP EMIF interface clock) to 245.76 MHz (the FPGA elaboration rate). Then the FPGA performs a number of other operations: a 2,048-point inverse fast Fourier transform, a cyclic prefix insertion, a PRACH data channel insertion, a half-shift function that translates the OFDM symbol spectrum at 7.5 kHz, a shaping and interpolation filtering and an intermediate-frequency (IF) conversion at 24 MHz. The device sends IF data to the DAC at a clock rate of 122.88 MHz. The radio card, meanwhile, converts the analog signal to RF and sends it to the transmitter amplifier.

In the downlink direction, after the LNA amplification, programmable-gain and conversion stages, the radio card will send IF received data to the SDR card (140 MHz). The ADCs subsample the analog data at 122.88 MHz and the FPGA handles the final 17.12-MHz frequency conversion to baseband. This data can be related either to two single-input, single-output channels or to one MIMO channel.

The IF data enters into the downlink FPGA, which converts it to baseband and then filters it. Polyphase decimation filters implement Nyquist filtering, spectrum image rejection and data-rate reduction at a symbol rate of 30.72 MHz, even though the chip rate remains at 245.76 MHz.

The FPGA incoming data flow looks like a stream of data instead of a series of OFDM symbols. The synchronization function slices the data stream properly to delineate the OFDM symbols. (To achieve this result, the synchronization circuit must detect Zadoff-Chu primary synchronization signals using multiple correlators on

deeply decimated input data. Afterwards, it will be possible to obtain OFDM symbols.) Finally, FFT transformation follows the removal of the cyclic prefix and the resulting data passes to another DSP using the EMIF interface.

The downlink flow involves two DSPs mutually connected by means of a serial RapidIO interface. These DSPs perform frequency correction, channel estimation, equalization and MIMO decoding. Then they do data- and control-channel extraction, Viterbi and turbo decoding, deinterleaving and descrambling prior to MAC-layer interworking.

On the uplink side, the third FPGA handles the loopback test between uplink and downlink FPGAs and ensures the SDR board's conformance to the CPRI/OBSAI standards.

Our design team extensively used Xilinx CORE Generator™ IP to produce filters, DDS, FFTs, Block RAMs, FIFOs and MACC functions, using DSP48E and DCMs for the clocking deskew section of

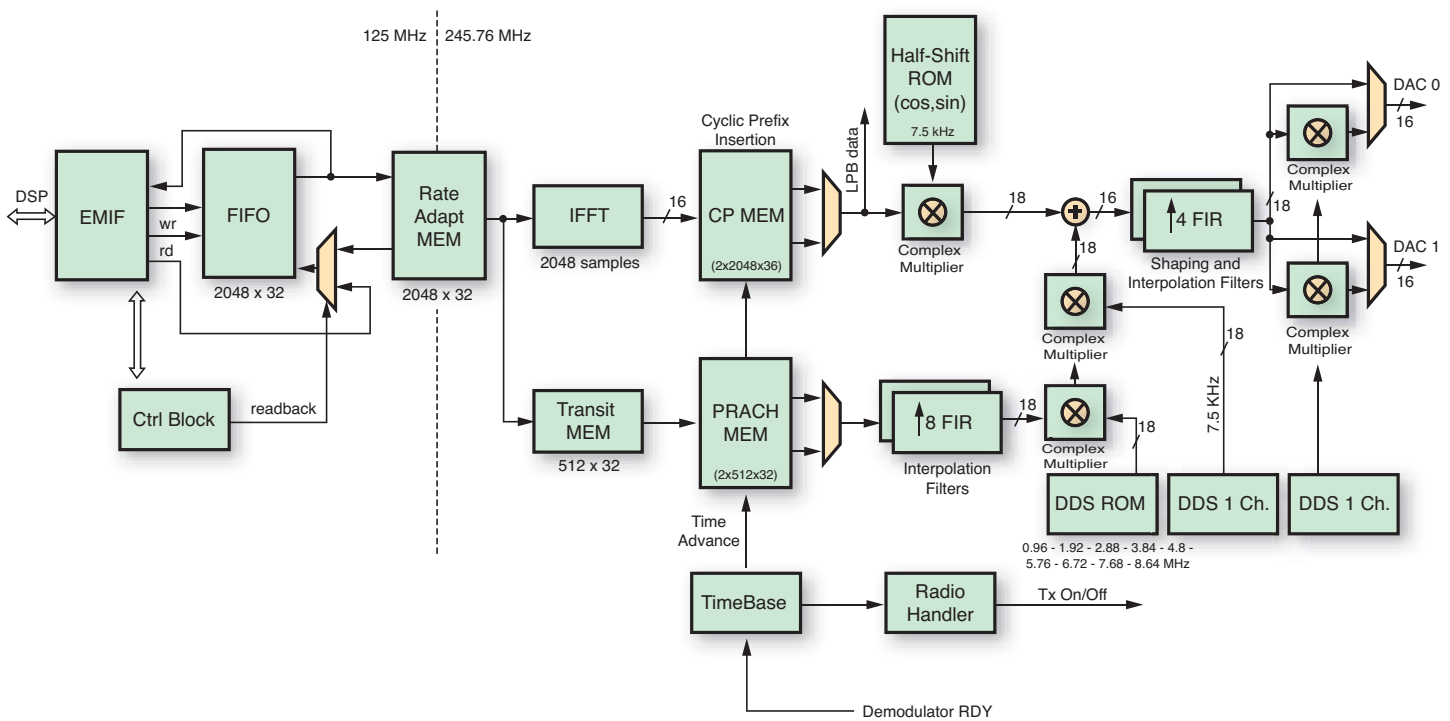


Figure 3 – The front-end “uplink FPGA” implements inverse FFT, IF upconversion and other operations for time-division duplex handling. The system sends the same signal into two DACs for redundancy.

Because this project had a very aggressive time-to-market deadline, we made a careful analysis of functions partitioning. The FPGAs would have accommodated even more LTE functions, but one of our design goals was to find a balance between the system's FPGA and DSP sections.

the design. This massive instantiation methodology produced a compact design in a reduced development time.

FPGA Design Strategy

Because this project had a very aggressive time-to-market deadline, our team made a careful analysis of functions partitioning among FPGAs and DSPs. It's worth noting that the FPGAs would have accommodated even more LTE functions, but one of our design goals was to find a balance between the FPGA and DSP sections of the system.

The FPGA clock rate was one of the tougher challenges in this design. Using a clock rate of 245.76 MHz for a large design

like a modulation system is not a trivial matter. Our design team had many issues to consider, such as power consumption, design constraints, placement and routing. Nevertheless, thanks to the ISE® Design Suite, which produced stable and quality results over the various design iterations, an oversampled factor of eight (FPGA clock rate/OFDM symbol rate) kept design items like filters and FFT transforms as small as possible with respect to the required LTE functionality. The ISE software also helped us achieve a reasonable synchronization circuit area.

Key to our design was devising a radio card architecture that in uplink, instead of

using a direct-conversion methodology with I/Q unbalance drawback, received the FPGA data from an intermediate frequency. Using Xilinx Direct Digital Synthesizers, an 18-bit sine/cosine wave performed a perfect signal carrier to the complex modulation, as confirmed by the error vector magnitude measured on the transmitted radio signal.

Thanks to the use of Xilinx Virtex-5 FPGA and TI DSP technologies, the LSU UeSIM LTE Simulator has become the leading-edge test equipment for load-and-stress solutions in the cellular world. It provides a powerful, flexible and scalable solution for SDR systems. 🌈

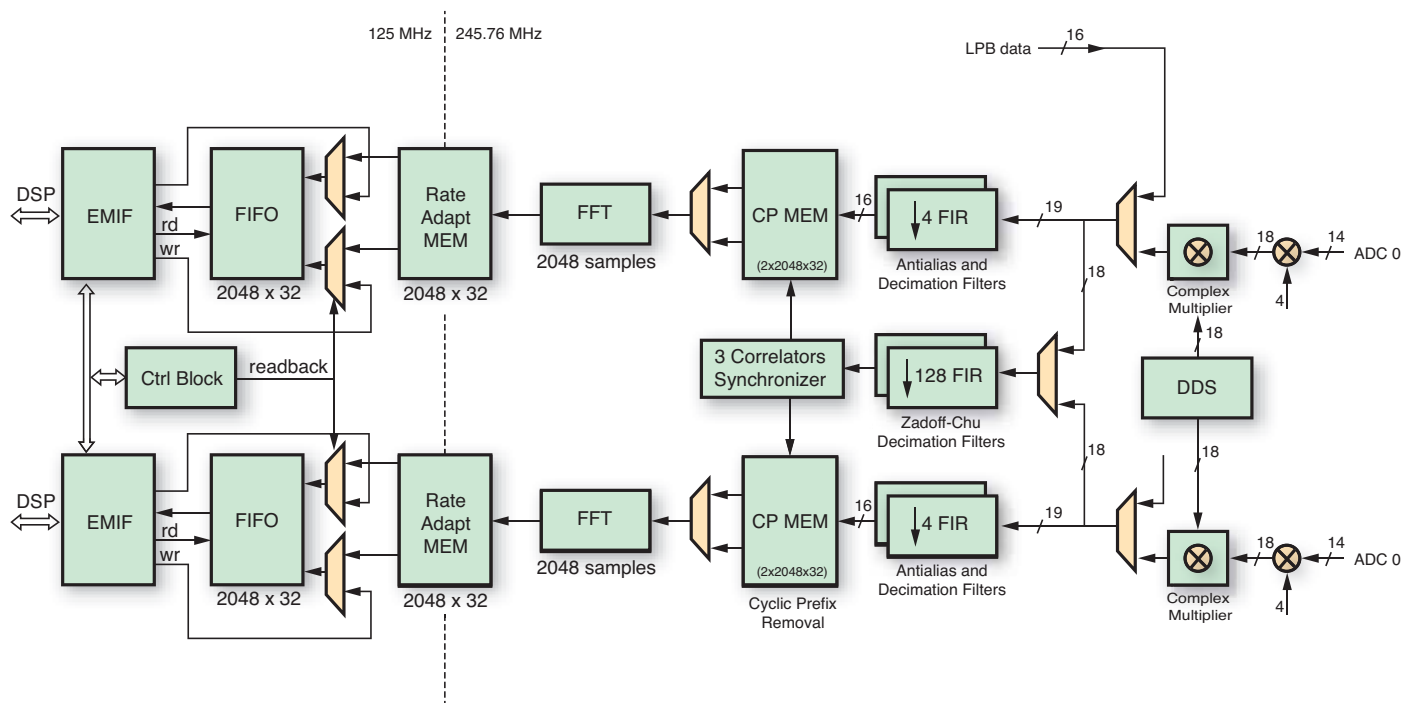


Figure 4 – The front-end “downlink FPGA” implements IF downconversion, polyphase decimation filtering, synchronization, cyclic prefix removal and direct FFT. The system uses two chains to support MIMO operations for TDD and FDD modes.